WR-109 WEATHER RADAR TEST SET

Giga-tronics

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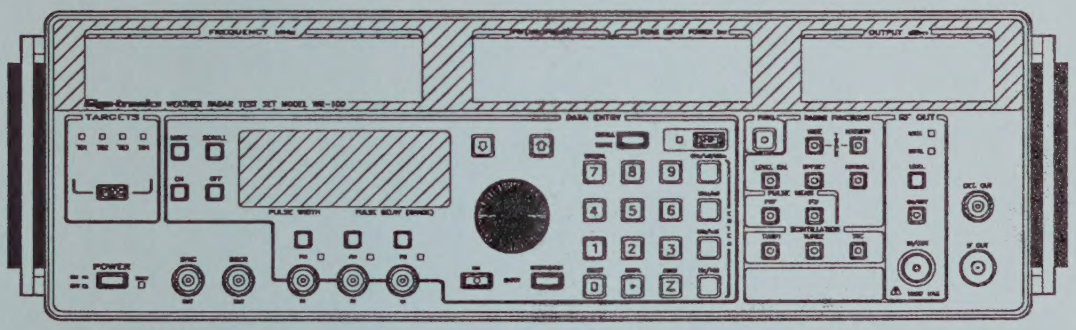
Giga-tronics

OPERATION & MAINTENANCE MANUAL

Series WR-100
Weather Radar Test Set

This manual applies to the WR-100 series (Models WR-103, WR-105, and WR-109). For information regarding model numbers, options, and instrument configurations, see page iii, Vol. 1.



Volume 2 of 2

Manual Part Number: 310AM17900
Print Date: December, 1992

Serial Numbers

The instrument has a five-digit serial number, which appears on a sticker on the rear panel. This manual applies to all serial numbers listed in Manual Changes (Section 10 of the manual; see Volume 2).

2495 ESTAND WAY ◆ P.O. BOX 232015 ◆ PLEASANT HILL, CALIFORNIA 94523-6015
PHONE (510) 680-8160 ◆ TELEX: ITT 4943689 ◆ FAX: (510) 680-7736

328-4650

WARRANTY

All Giga-tronics instruments are warranted against defective materials and workmanship for three years from date of shipment. Giga-tronics will at its option repair or replace products that are proven defective during the warranty period.

This warranty DOES NOT cover damage resulting from improper use, nor workmanship other than Giga-tronics service.

There is no implied warranty of fitness for a particular purpose, nor is Giga-tronics liable for any consequential damages.

Specification and price change privileges are reserved by Giga-tronics.

SYMBOLS

Block diagram symbols frequently used in the manual are illustrated below.

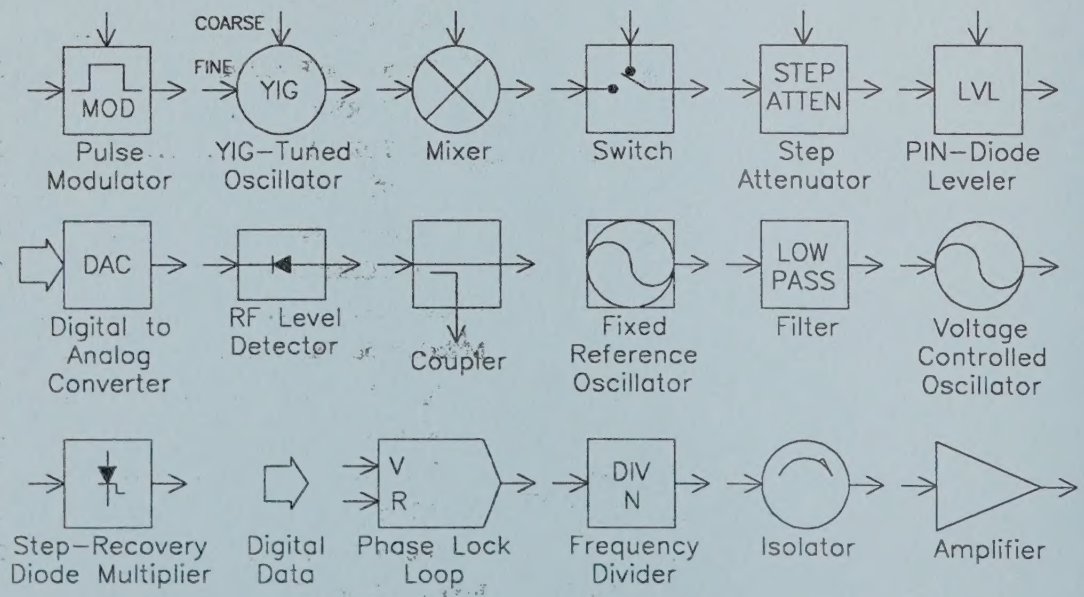


TABLE OF CONTENTS

VOLUME 1

Intro & Performance Specifications 1

Manual Information 1-1
Introduction 1-2
- Purpose and Function 1-2
- Performance Characteristics 1-2
- Weight and Dimensions 1-2
- Power Requirements 1-2
- Environmental Requirements 1-2
- Items Furnished 1-2
- Items Required 1-2
- Tools and Test Equipment 1-2
- Storage 1-2
- Cooling 1-2
- Cleaning 1-3
- Installation & Preparation for Use 1-3
- Receiving Inspection 1-3
- Preparation for Reshipment 1-3
- Safety Precautions 1-4
- Voltage Selection 1-5
- Fuse Selection 1-5

Performance Specifications 1-6
- Tracking Counter/Generator Characteristics 1-6
- IF Range Output 1-6
- Spectral Purity 1-6
- Output Power Characteristics 1-6
- Input Power Measurement 1-7
- Pulse Modulation Characteristics 1-7
- Multiple Targets 1-7
- External AM Characteristics 1-7
- External FM Characteristics 1-8
- Scintillation 1-8
- Inputs 1-8
- Outputs 1-9
- Environmental 1-9
- General Specifications 1-9

Operational Information 2

Front Panel 2-1
- Key Interpretation 2-2
- Operating Modes 2-2
- Numeric Data Entry 2-2
- Data Entry Resolution 2-3
- Entry Disable 2-3
- Shifted Functions 2-3
- Store/Recall 2-3

Generate Mode 2-4
- Frequency Setting 2-4
- Level Setting 2-5
- Pulse Modulation 2-6
  - Internal Pulse Modulation 2-6
  - External Pulse Modes 2-7
  - External Trigger Modes 2-7
- Amplitude Modulation 2-8
- Frequency Modulation 2-8
- IF Sweep 2-8

Track Modes 2-9
- Frequency Offset 2-9
- Pulse Measurement 2-10
- Scintillation Functions 2-11
  - TURB 1 2-11
  - TURB 2 2-12
  - STC 2-12
- Multiple Targets 2-13
- Level Calibration 2-14

Manual Mode 2-15
Miscellaneous Functions 2-16
- Special 2-16
- Reset 2-16
- Local 2-16
- ADRS 2-16
- Special Functions Table 2-17

Input and Output Connectors 2-18

TABLE OF CONTENTS

Rear Panel 2-19
Rear Panel Connectors 2-19
Line Power and Fuse Section 2-19
Interface Section 2-20
Remote Control Interface 2-21
Interface Hardware Configuration 2-21
Address Assignment 2-22
Command Interpretation 2-22
Giga-tronics Remote Programming Syntax ... 2-23
Character Representation 2-23
Command Format 2-23
Commands 2-24
STC Patterns 2-27

Theory of Operation ***3***

General Configuration of the Instrument 3-1
The Computer 3-2
Microwave Frequency Synthesis 3-3
Phase Lock Loops 3-3
Reference Branch 3-5
Variable Branch 3-9
IF Output 3-12
Amplitude Control 3-13
ALC Loop 3-13
Modulation 3-14
Frequency Modulation 3-14
Amplitude Modulation 3-14
Pulse Modulation 3-14
Scintillation 3-15
Frequency Measurement 3-17
Pulse Measurement and Modulation; Power Measurement 3-18

Calibration and Testing ***4***

Warm-up Time 4-1
Required Test Equipment 4-2
Calibration/Test Frequencies 4-2
Calibration Procedure 4-3
VCO Driver 4-3
Downconverter PLL 4-3
Level 4-3
Multiple Target Amplitude 4-3
Amplitude Modulation 4-4
Frequency Modulation 4-4
IF Sweep Ramp 4-4
Timebase 4-4
Discriminator 4-5
Peak Power Offset 4-5
Performance Tests 4-7
RF Frequency Accuracy 4-7
RF Frequency Range 4-7
Output Power Accuracy 4-7
IF Frequency Range 4-7
IF Output Power 4-7
IF Sweep Ramp 4-7
Spurious/Attenuator Test 4-8
On/Off Ratio 4-8
Pulse Modulation (Single Target) 4-8
Int PM 4-9
Ext Trig 4-9
Pulse Modulation (Multiple Targets) 4-9
RF Counter Accuracy 4-10
Tracking Accuracy 4-10
Power Meter Accuracy 4-10
Pulse Repetition Freq/Pulse Width Test .. 4-12
Discriminator Output Accuracy 4-12
Scintillation Functions 4-12
Amplitude Modulation Functions 4-13
Frequency Modulation Functions 4-13
Miscellaneous Functions 4-13
Model WR-103 Test Data Sheet 4-14
Model WR-105 Test Data Sheet 4-18
Model WR-109 Test Data Sheet 4-22

Maintenance ***5***

Safety Precautions 5-1
Preliminary Troubleshooting 5-1

TABLE OF CONTENTS

Failure Analysis 5-2
General Failure 5-2
Loss of RF Output 5-2
Incorrect Output Level 5-2
Output Frequency Unlocked 5-3
Output Locked, but Frequency Incorrect 5-3
Pulse Modulation Malfunction 5-3
Scintillation Malfunction 5-4
Freq Counter/Tracking Malfunction 5-4
PRF/PW Counter Malfunction 5-4
Peak Power Meter Malfunction 5-4
IEEE-488 Interface Malfunction 5-4
Troubleshooting Notes 5-5
Power Supplies 5-5
Computer 5-6
10 dB Step Attenuator 5-6
Pulse Modulator 5-6
Output VCO 5-7
Leveler 5-7
Detector 5-7
Level Control Circuit 5-8
Individual PLL Lock Indicators 5-8
Output Phase Lock Loop 5-8
Divide-by-N Circuit 5-9
300 MHz Oscillator 5-9
300 MHz Phase Lock Loop 5-9
VCO Driver 5-9
Oscillator/Multiplier 5-10
110 MHz PLL 5-10
10 MHz Master Reference 5-10
Divide-By-8 Circuit 5-10
40-80 MHz Phase Lock Loop 5-11
Modulator 5-11
Multi-Target Digital Pulse Gen, Driver 5-11
Scan Modulation 5-12
IF Counter 5-12
Downconverter 5-13
PRF A/D Peak Detector 5-13
GPIB Address 5-14
Remote Commands 5-14
IEEE-488 Interface Circuit 5-14
Preventive Maintenance 5-15
Disassembly, Repair, Replacement & Reassembly 5-15

Parts Lists ***6***

Basic Unit Asy 6-1
Front Panel Asy 6-3
Opt Encoder Harness Asy 6-3
Pushbutton Switch Assemblies 6-4
Rear Panel 6-5
4 Conn Plate WR100 Asy 6-5
RF Deck RT1009 Asy 6-5
Heatsink Asy 6-6
Fan Asy 6-7
Computer Chassis Asy 6-8
Bench Mount Dress 6-9
Bottom Cover Asy 6-9
Handle Asy 6-9
M6XXX Rack Mount 6-10
M6XXX Rack Mount/Slides 6-10
Accessories WR100 Asy 6-10
Freq 2.4-3.7 WR103 Asy 6-11
Delay Line RT1009 Asy 6-12
Sampler Asy 6-13
VCO Module WR103 Asy 6-13
3.0 Pulse/Scan WR103 Asy 6-13
3.0 Coupler WR103 Asy 6-13
M-Switch WR100 MWA 6-13
3.0 LM Mod WR103 Asy 6-14
3.0 Combiner WR103 Asy 6-14
3.0 Cplr/Det WR103 Asy 6-14
3.0 Peak/Cplr WR103 Asy 6-14
Sampler Assembly 6-14
Downconverter WR103 Asy 6-14
Dnconv LO WR103 PCA 6-15
Downconv Amplifier PCA 6-15

TABLE OF CONTENTS

Sampler Driver WR100 PCA 6-15
Sampler LF. PCA 6-16
Freq 9.0-9.5 WR109 Asy 6-17
Sampler Assembly 6-18
VCO Module RT1009 Asy 6-18
9.3 Pulse/Scan WR100 MWA 6-18
9.3 Coupler 30 WR100 Asy 6-19
M-Switch WR100 MWA 6-19
9.3 LM Module WR100 MWA 6-19
9.3 Combiner WR100 MWA 6-19
9.3 Coupler WR100 MWA 6-19
Downconverter WR109 Asy 6-20
Sampler Assembly 6-20
Downconv LO WR100 PCA 6-20
Down Conv. Amplifier PCA 6-20
Sampler Driver WR100 PCA 6-21
Sampler LF. PCA 6-22
VIA PCA (A0) 6-23
Keyboard/LED VIA PCA (A1) 6-24
Memory PCA (A2) 6-25
Fast IEEE PIA PCA (A3) 6-27
Dual Microproc CPU (A4) 6-28
Level Control PCA (A5) 6-30
Output PLL/Hold PCA (A6) 6-33
Divider PCA (A7) 6-36
40-80 MHz PLL PCA (A8) 6-38
Intermediate PLL PCA (A9) 6-40
Hi Resolution PCA (A10) 6-43
300 MHz PLL PCA (A11) 6-45
110 MHz Ref PLL PCA (A12) 6-47
VCO Driver PCA (A13) 6-49
Driver PCA (A14) 6-51
Multi Target Generator PCA (A15) 6-54
Scan Modulation PCA (A16) 6-57
PRF A/D Peak Detector PCA (A17) 6-60
IF Counter PCA (A18) 6-63
Display Driver PCA (A20) 6-65
TCXO PCA (A32) 6-67
Power Supply PCA (A101) 6-67
RF Bus PCA (A102) 6-68
11 Digit Display PCA (A103) 6-68
5 & 9 Digit Display PCA (A104) 6-68
Push Button PCA (A105) 6-69
Data Entry PCA (A106) 6-70
Computer Bus PCA (A110) 6-72
Modulation Bus PCA (A112) 6-72
Discrim Amp PCA (A114) 6-73
Pulse Profile PCA (A115) 6-75
IF Switch PCA (A116) 6-76
Downconverter PLL PCA (A118) 6-77
Oscillator/Multiplier PCA (A201) 6-80
300 MHz Oscillator PCA (A202) 6-82
Detector Buffer PCA (A212) 6-85
List of Manufacturers 6-87

VOLUME 2

Diagrams ***7***

WR-100 Input/Output Block Diagram 7-1
WR-100 RF Block Diagram 7-2
Basic Unit 7-3
Front Panel Assy 7-6
Computer Chassis Assy 7-8
Heatsink Assy 7-10
Power Supply Assy 7-11
Rear Panel Assy 7-12
RF Deck Assy 7-13
Frequency 9.0-9.5 WR-109 Assy 7-14
Frequency 2.4-3.7 WR-103 Assy 7-18
VIA PCA (A0) 7-A0-1
Keyboard/VIA PCA (A1) 7-A1-1
Memory PCA (A2) 7-A2-1
Fast IEEE PCA (A3) 7-A3-1
Dual Microprocessor CPU (A4) 7-A4-1
Level Control PCA (A5) 7-A5-1
Output PLL PCA (A6) 7-A6-1
Divider PCA (A7) 7-A7-1

TABLE OF CONTENTS

40-80 MHz PLL PCA (A8) 7-A8-1
Intermediate PLL PCA (A9) 7-A9-1
High Resolution PCA (A10) 7-A10-1
300 MHz PLL PCA (A11) 7-A11-1
110 MHz Ref PLL PCA (A12) 7-A12-1
VCO Driver PCA (A13) 7-A13-1
Driver PCA (A14) 7-A14-1
Multi Target Generator PCA (A15) 7-A15-1
Scan Modulation PCA (A16) 7-A16-1
PRF A/D Peak Detector PCA (A17) 7-A17-1
IF Counter PCA (A18) 7-A18-1
Display Driver PCA (A20) 7-A20-1
TCXO PCA (A32) 7-A32-1
Power Supply PCA (A101) 7-A101-1
RF Bus PCA (A102) 7-A102-1
11 Digit Display PCA (A103) 7-A103-1
5 & 9 Digit Display PCA (A104) 7-A104-1
Push Button PCA (A105) 7-A105-1
Data Entry PCA (A106) 7-A106-1
Computer Bus PCA (A110) 7-A110-1
Modulation Bus PCA (A112) 7-A112-1
Discriminator Amp PCA (A114) 7-A114-1
Pulse Profile PCA (A115) 7-A115-1
IF Switch PCA (A116) 7-A116-1
Downconverter PLL PCA (A118) 7-A118-1
Oscillator/Multiplier PCA (A201) 7-A201-1
300 MHz Oscillator PCA (A202) 7-A202-1
Detector Buffer PCA (A212) 7-A212-1

Options ***8***

Option 05: Beacon Test 8-2

Special Configurations ***9***

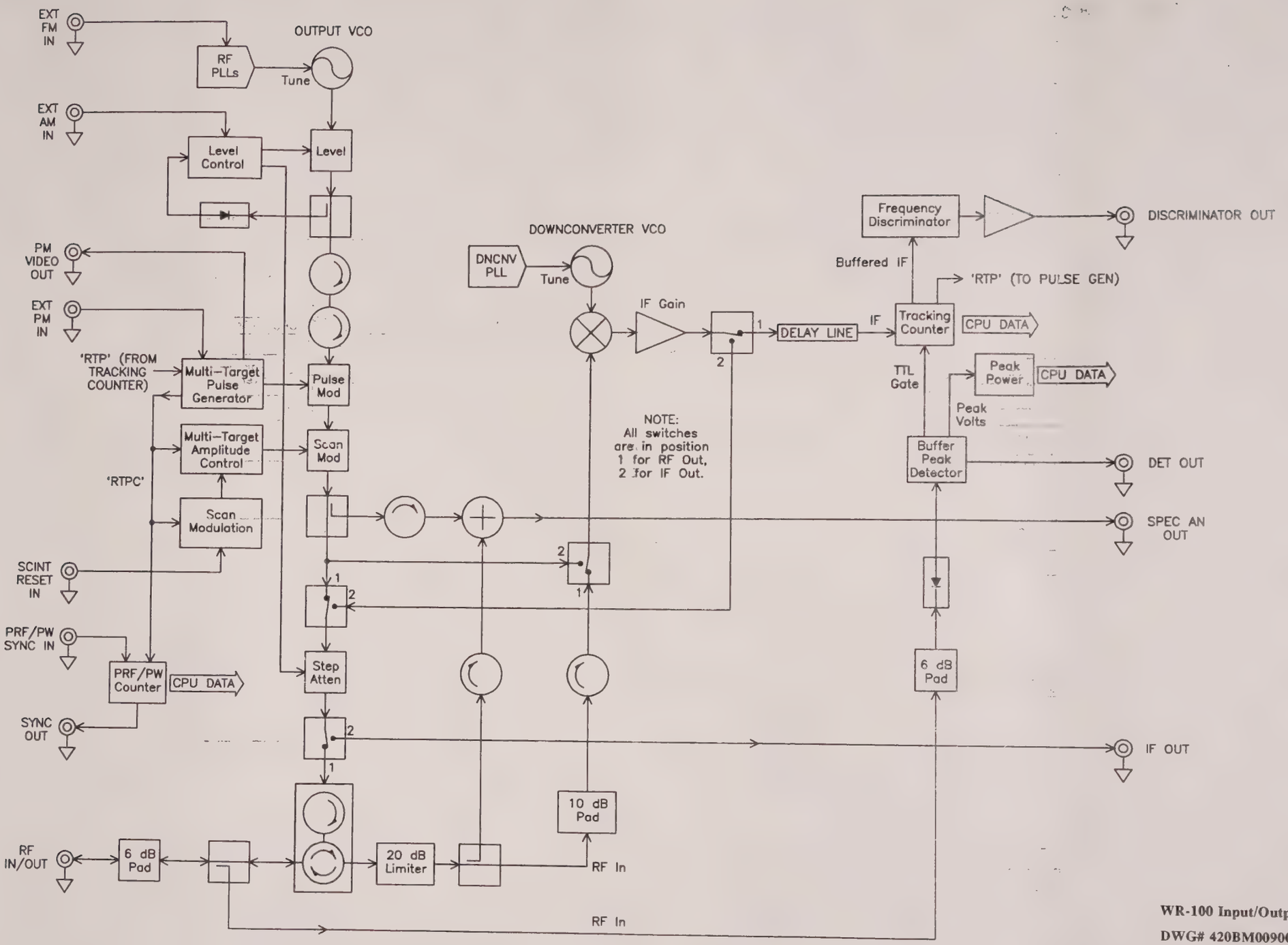
Manual Changes ***10***

Reserved for post-publication changes made to this manual

List of Illustrations

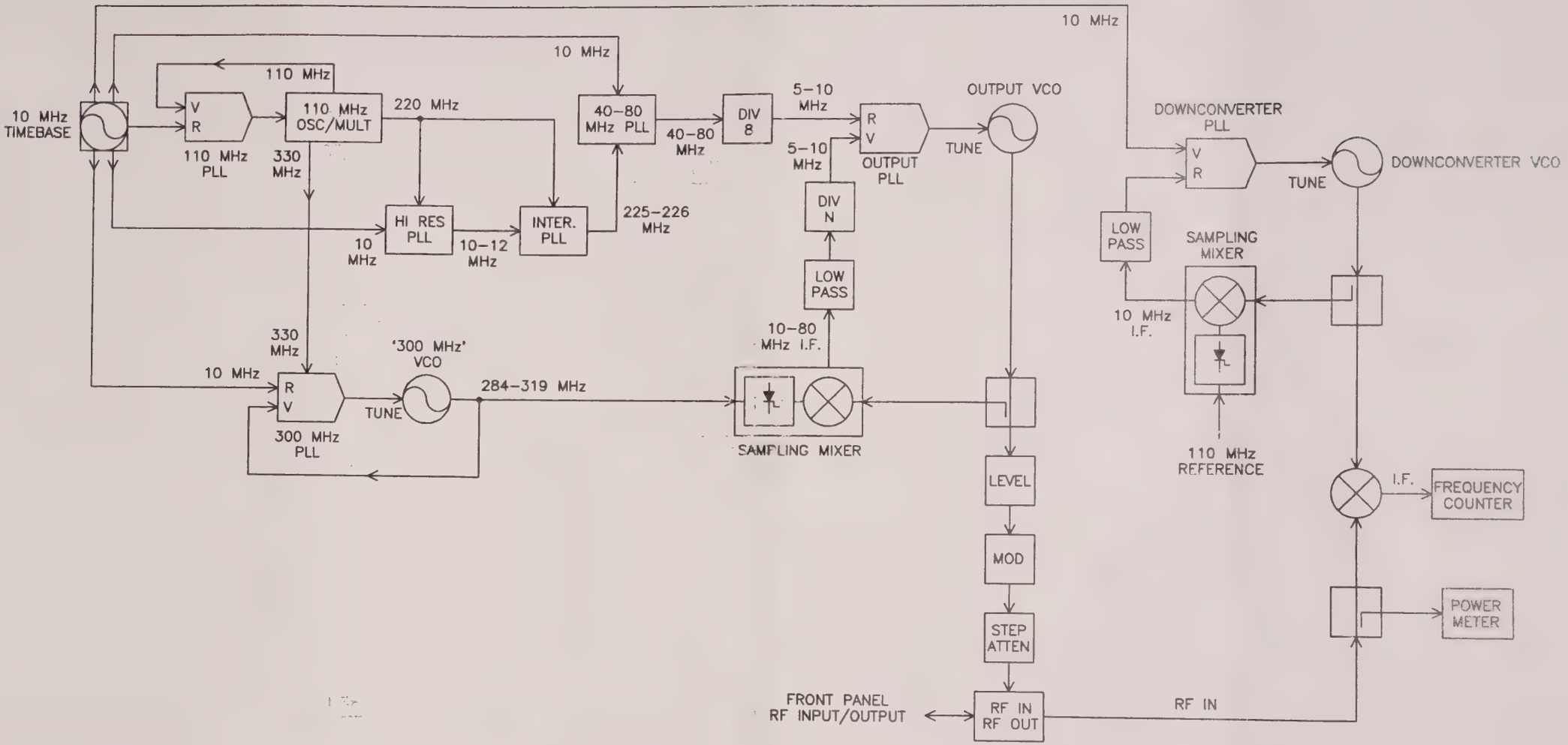
Fig. 1.1: Power Line Connection 1-4
Fig. 1.2: Voltage Selector/Fuse Holder 1-5
Fig. 2.1: Front Panel 2-1
Fig. 2.2: Front Panel Operation 2-3
Fig. 2.3: Generate Mode 2-4
Fig. 2.4: Level Setting 2-5
Fig. 2.5: Pulse Modulation (Internal) 2-6
Fig. 2.6: External Pulse Modulation 2-7
Fig. 2.7: AM, FM, and IF Sweep 2-8
Fig. 2.8: Track Mode 2-9
Fig. 2.9: Pulse Measurement 2-10
Fig. 2.10: Turbulence Functions 2-11
Fig. 2.11: STC Functions 2-12
Fig. 2.12: Multiple Targets 2-13
Fig. 2.13: Level Cal 2-14
Fig. 2.14: Manual Mode 2-15
Fig. 2.15: Miscellaneous Functions 2-16
Fig. 2.16: Front Panel Connectors 2-18
Fig. 2.17: Rear Panel 2-19
Fig. 3.1: WR-100 Internal Layout 3-1
Fig. 3.2: Computer 3-2
Fig. 3.3: Phase Lock Loop 3-3
Fig. 3.4: Phase Lock Loop, with Prescaler 3-4
Fig. 3.5: Reference Branch 3-5
Fig. 3.6: 110 MHz Oscillator/Multiplier & PLL 3-6
Fig. 3.7: High Resolution PLL 3-7
Fig. 3.8: Intermediate PLL 3-7
Fig. 3.9: 40-80 MHz PLL 3-8
Fig. 3.10: Variable Branch 3-9
Fig. 3.11: 300 MHz PLL & VCO 3-10
Fig. 3.12: Sampling Mixer & Output PLL 3-11
Fig. 3.13: Downconverter Circuit 3-12
Fig. 3.14: ALC Circuit 3-13
Fig. 3.15: Modulation 3-14
Fig. 3.16: Turbulence Functions 3-15
Fig. 3.17: STC Function 3-16
Fig. 3.18: Frequency Measurement 3-17

Fig. 3.19: Pulse & Power Measurement 3-18



WR-100 Input/Output Block Diagram

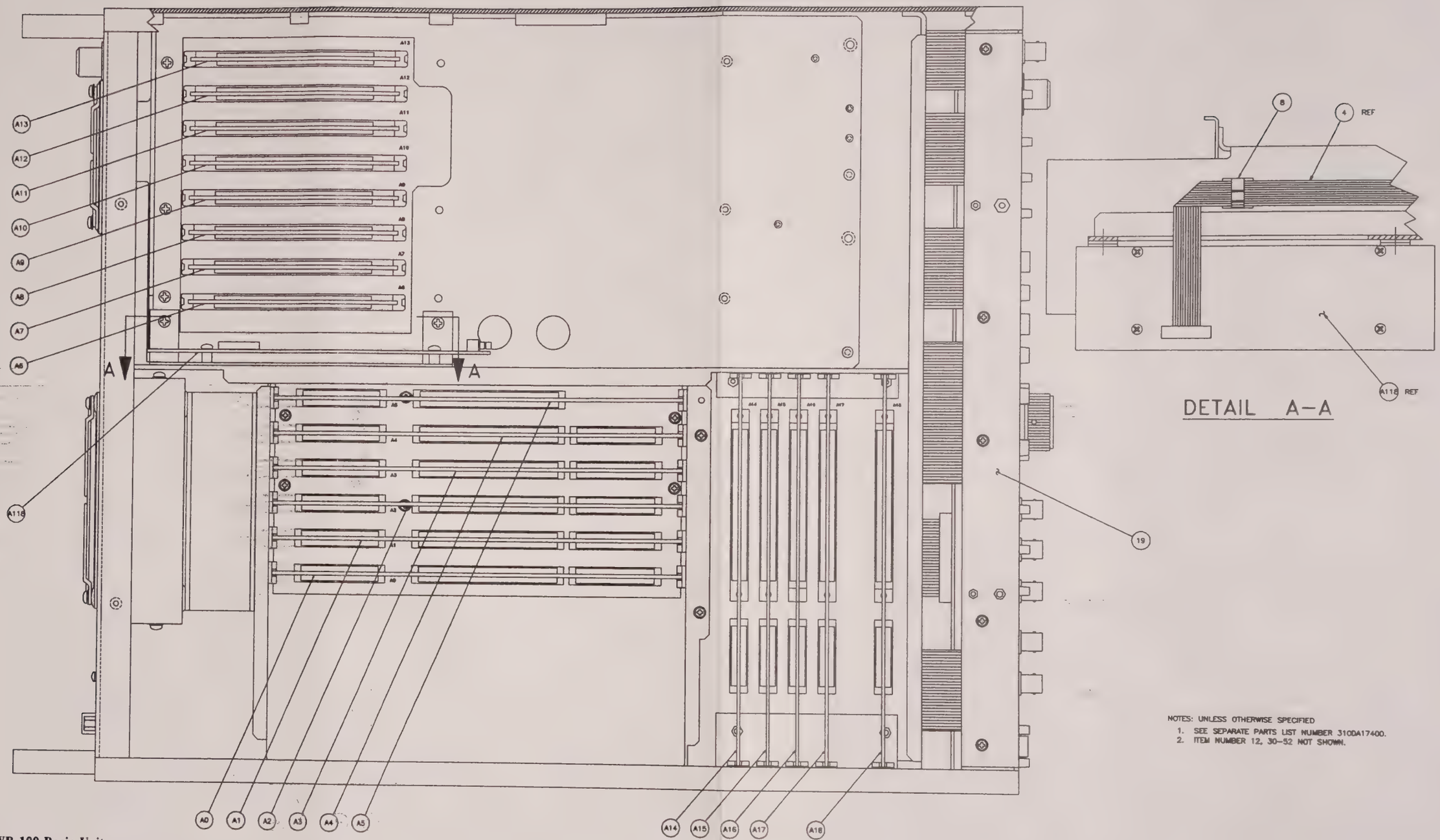
DWG# 420BM00900 Rev A



WR-100 RF Block Diagram

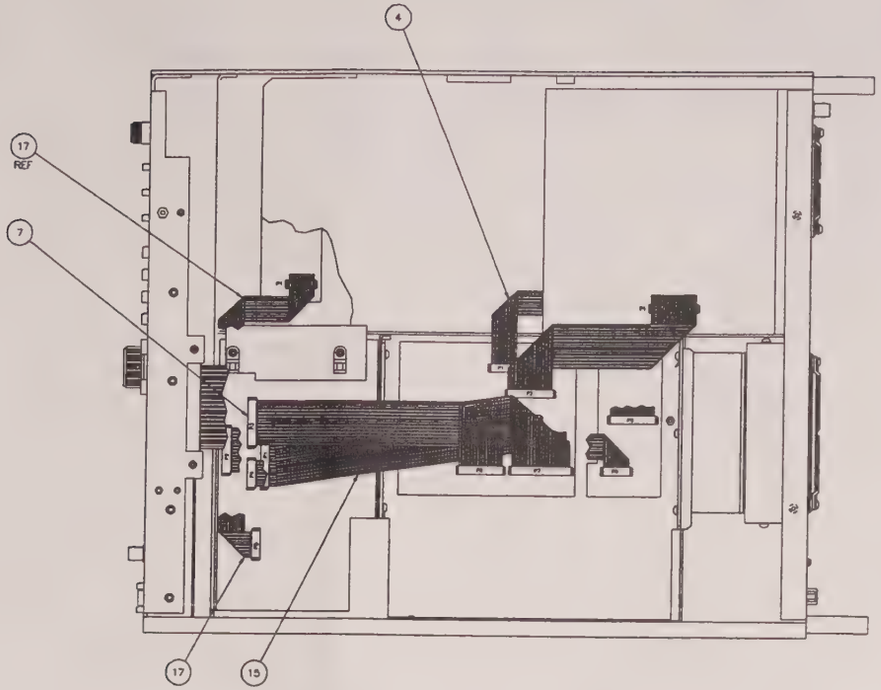
DWG# 420BM02600 Rev A

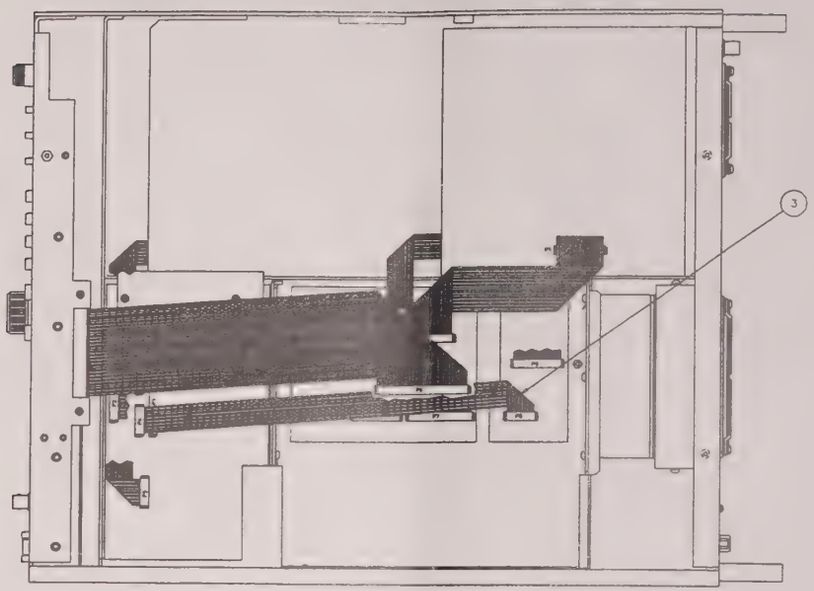
Sheet 1 of 1



NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SEPARATE PARTS LIST NUMBER 310DA17400.
2. ITEM NUMBER 12, 30–32 NOT SHOWN.


4
17
REF
7
17
15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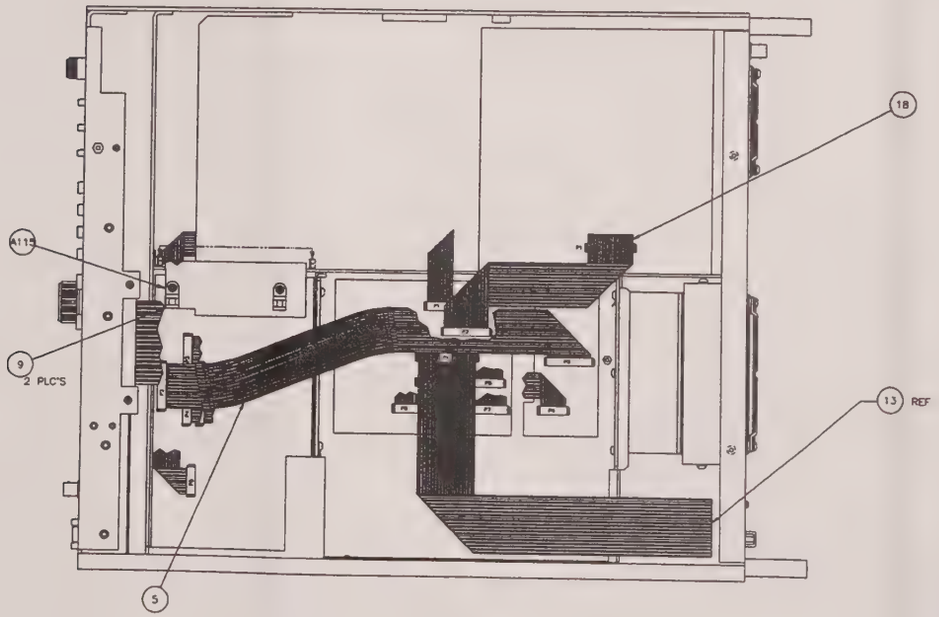
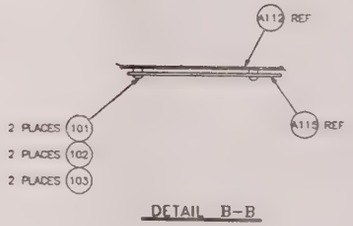
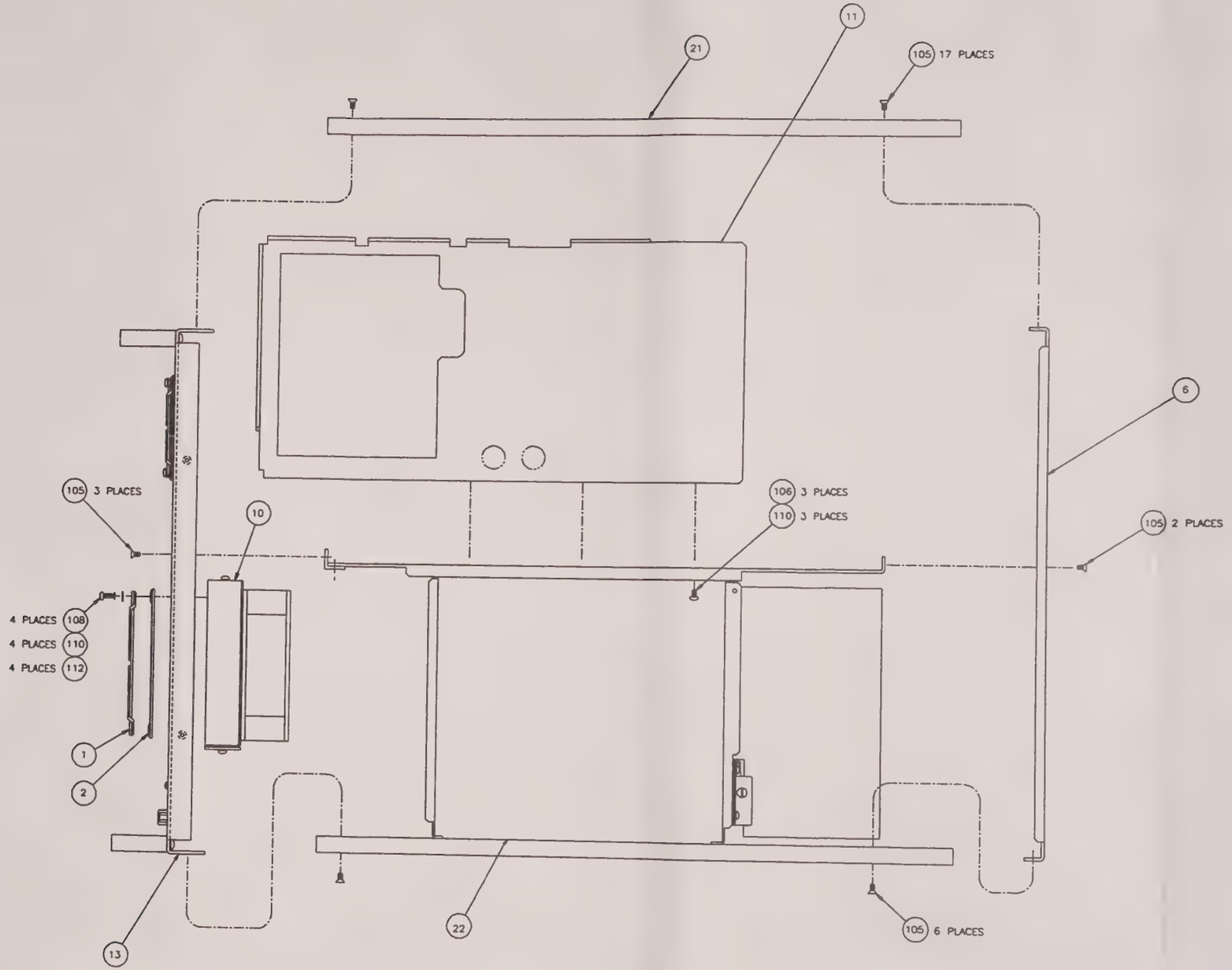

18
A112
9
2 PLC'S
13
REF
5


A112
REF
2 PLACES
101
2 PLACES
102
2 PLACES
103
A115
REF

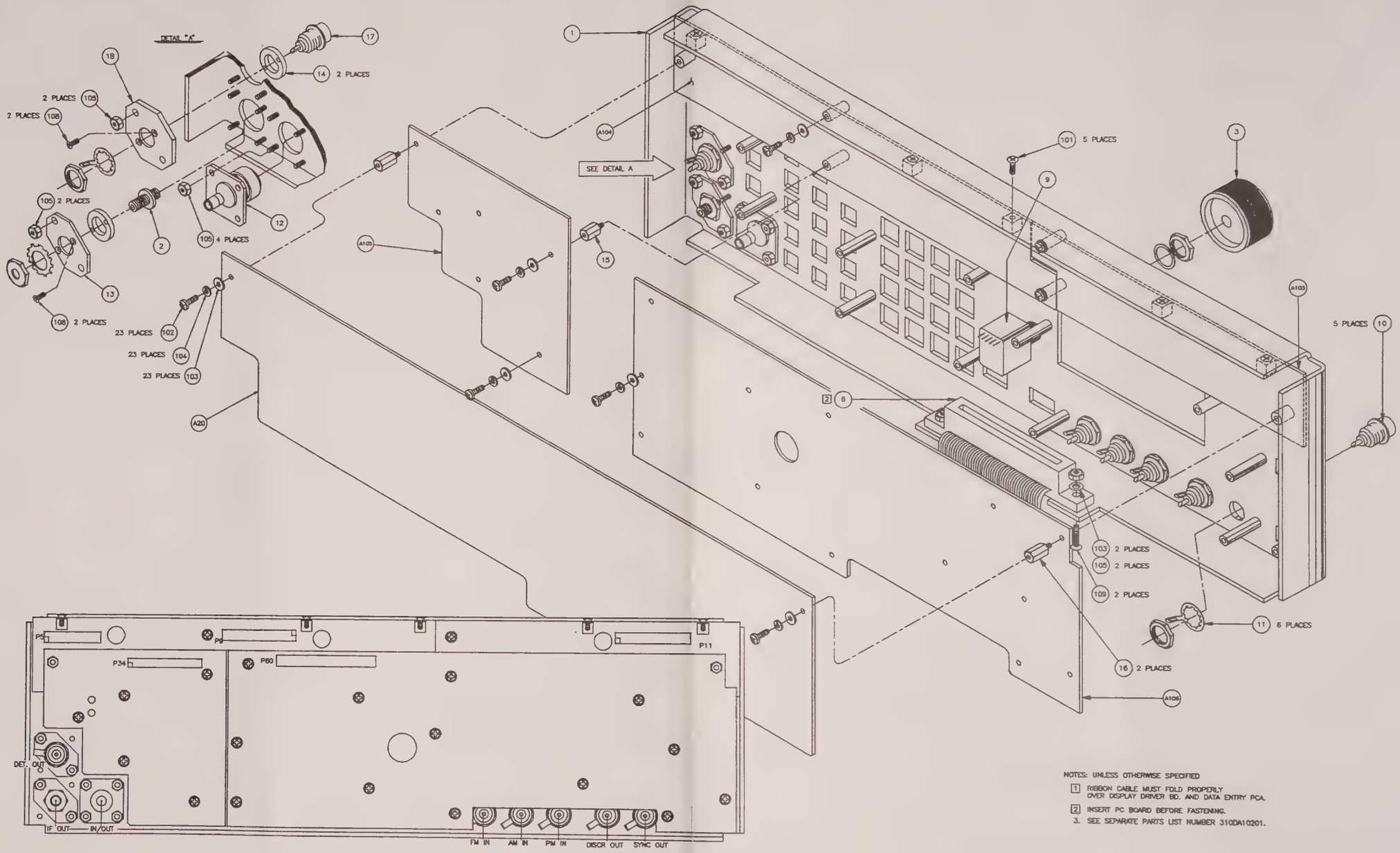
DETAIL B-B



WR-100 Basic Unit

DWG# 310BM17400 Rev D

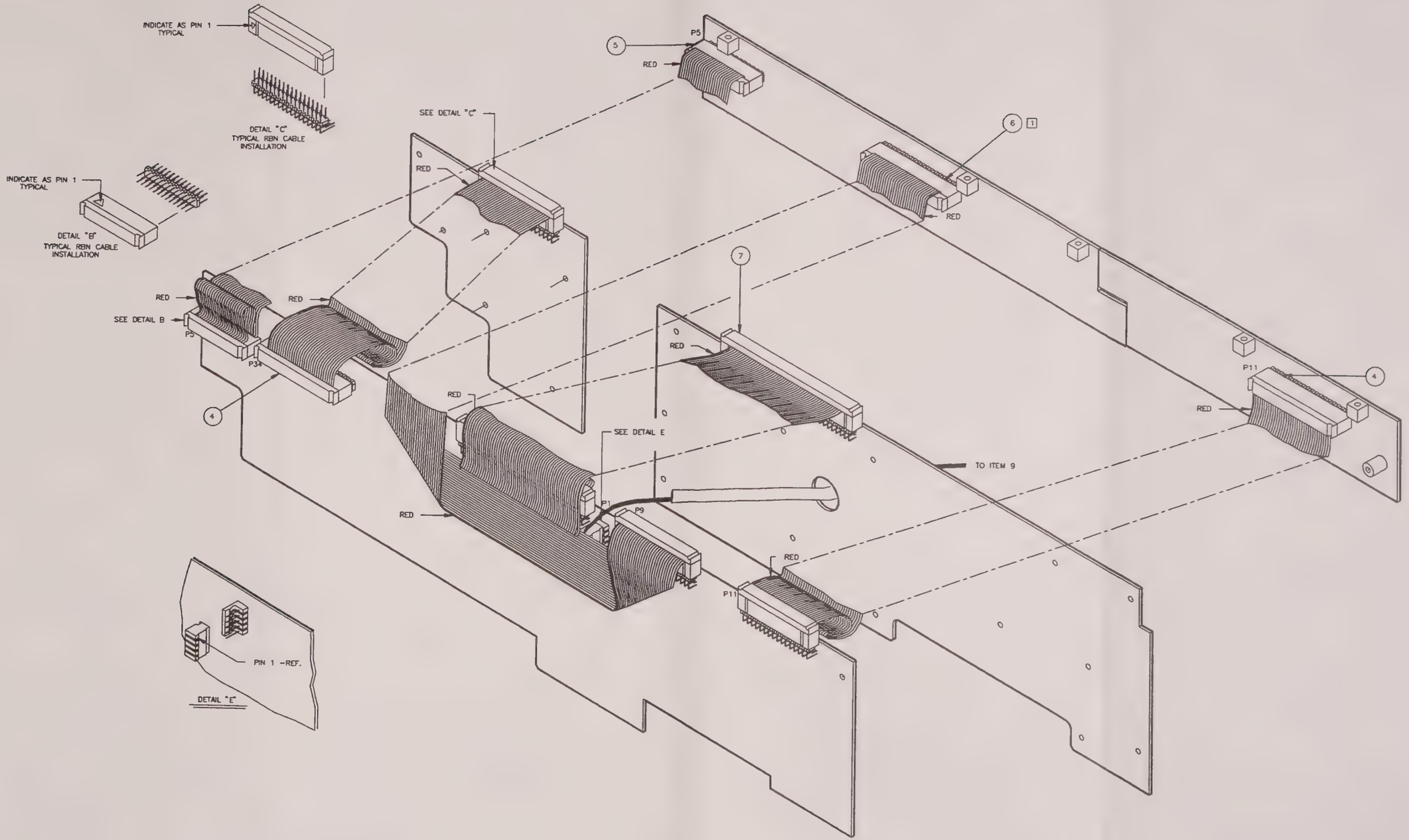
Sheet 3 of 3



Front Panel Assy

DWG# 310BM10201 Rev A

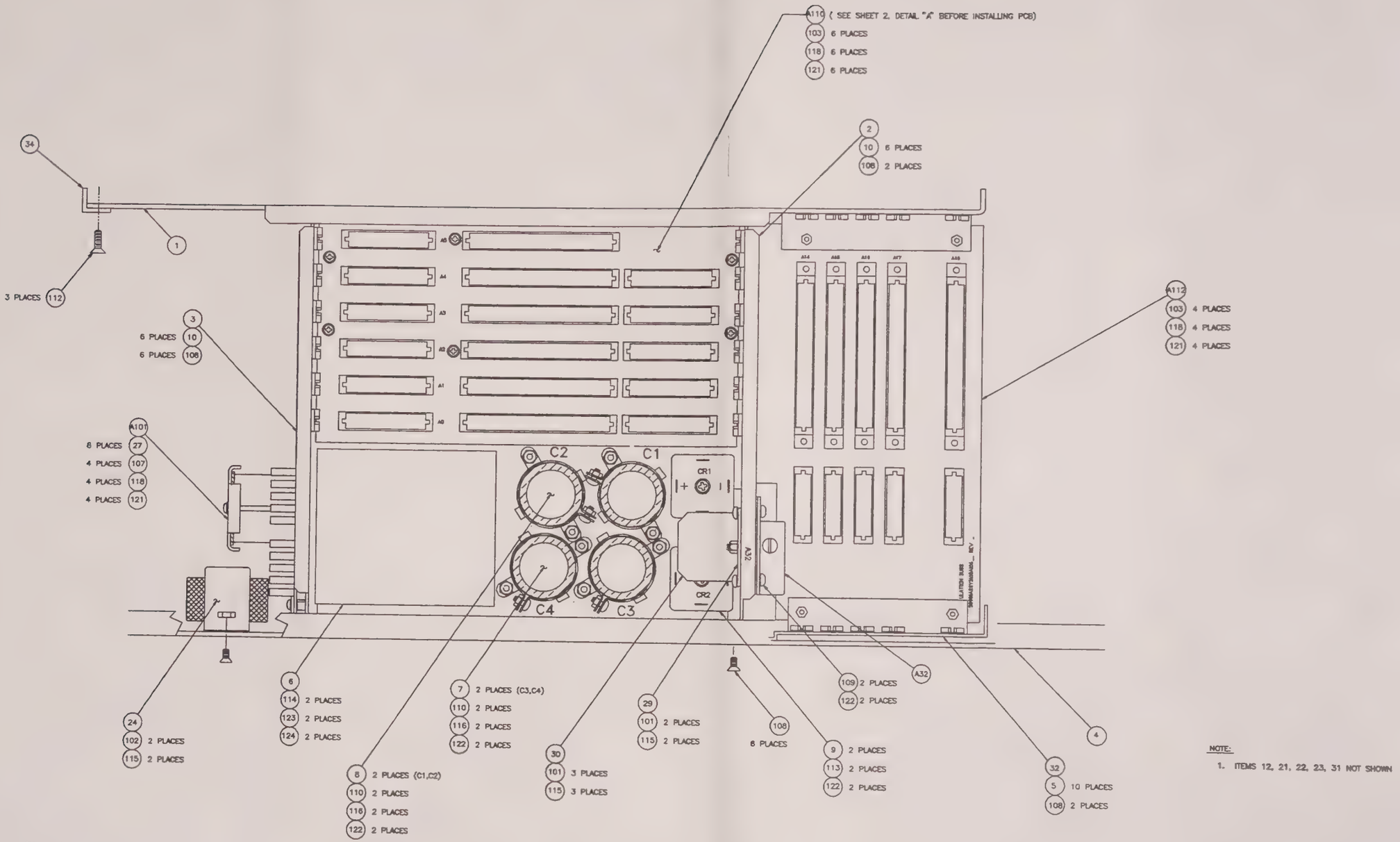
Sheet 1 of 2



Front Panel Assy

DWG# 310BM10201 Rev A

Sheet 2 of 2



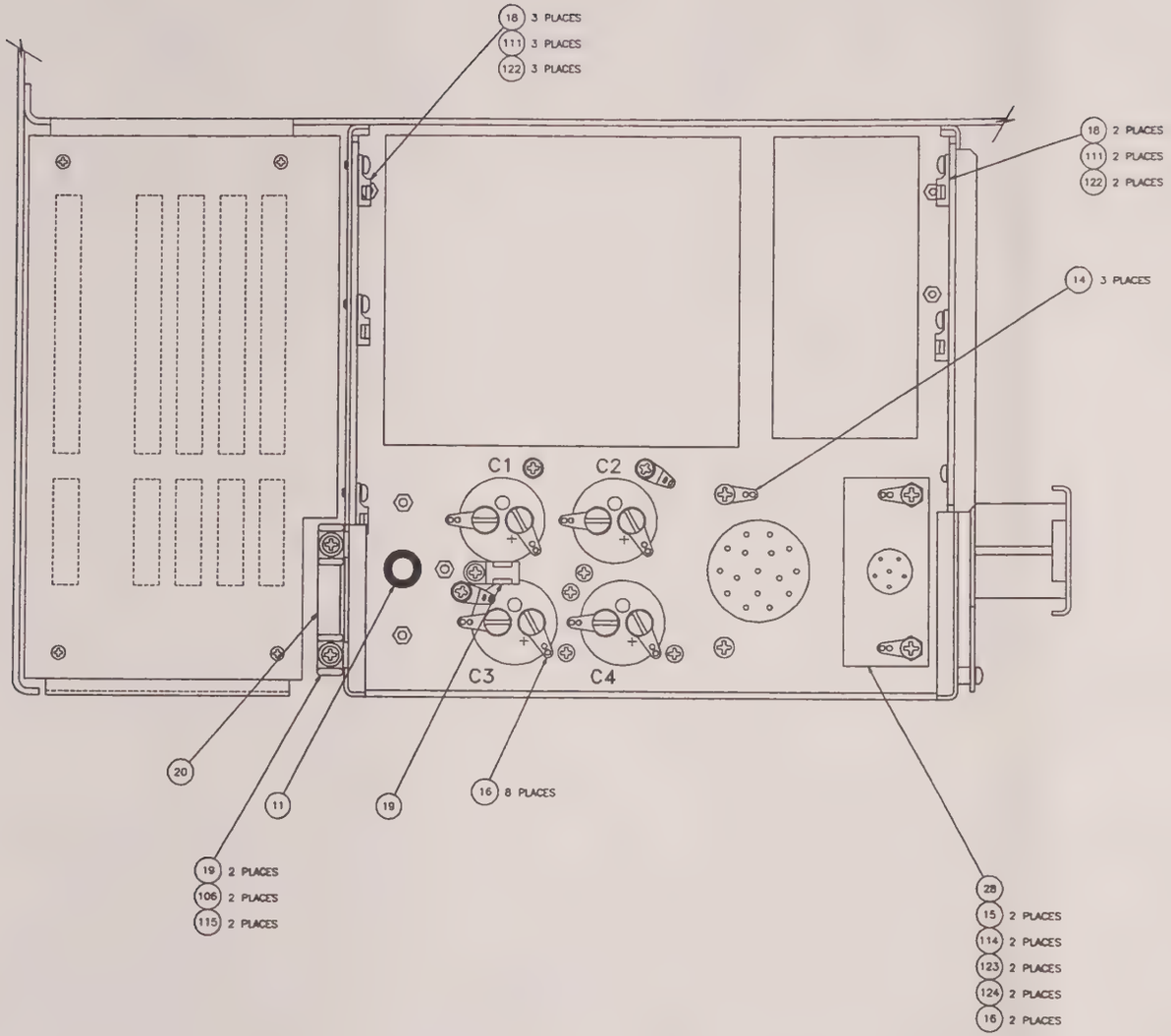
NOTE:

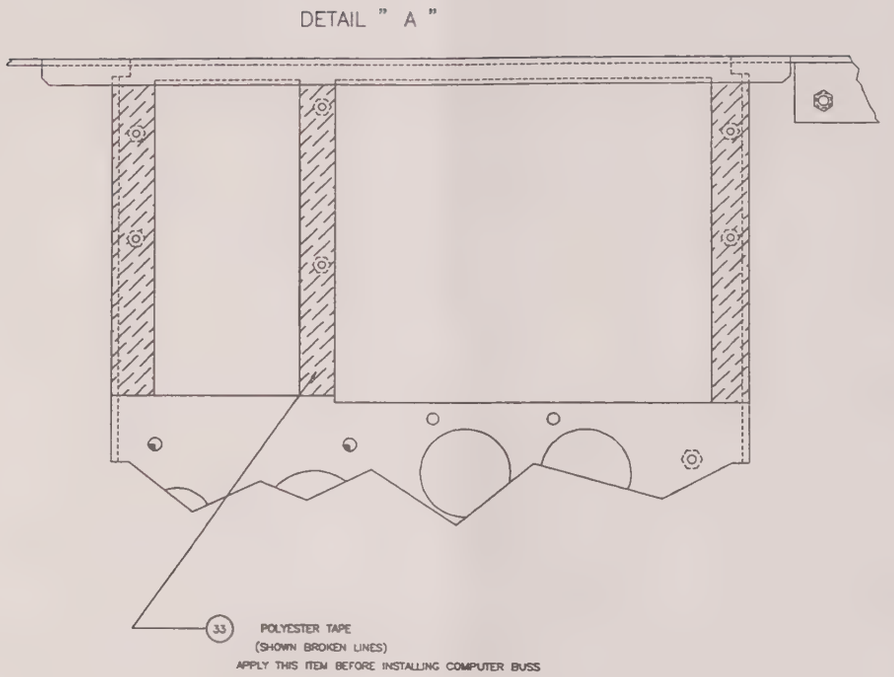
1. ITEMS 12, 21, 22, 23, 31 NOT SHOWN

Computer Chassis Assy

DWG# 310BM16501 Rev D

Sheet 1 of 2

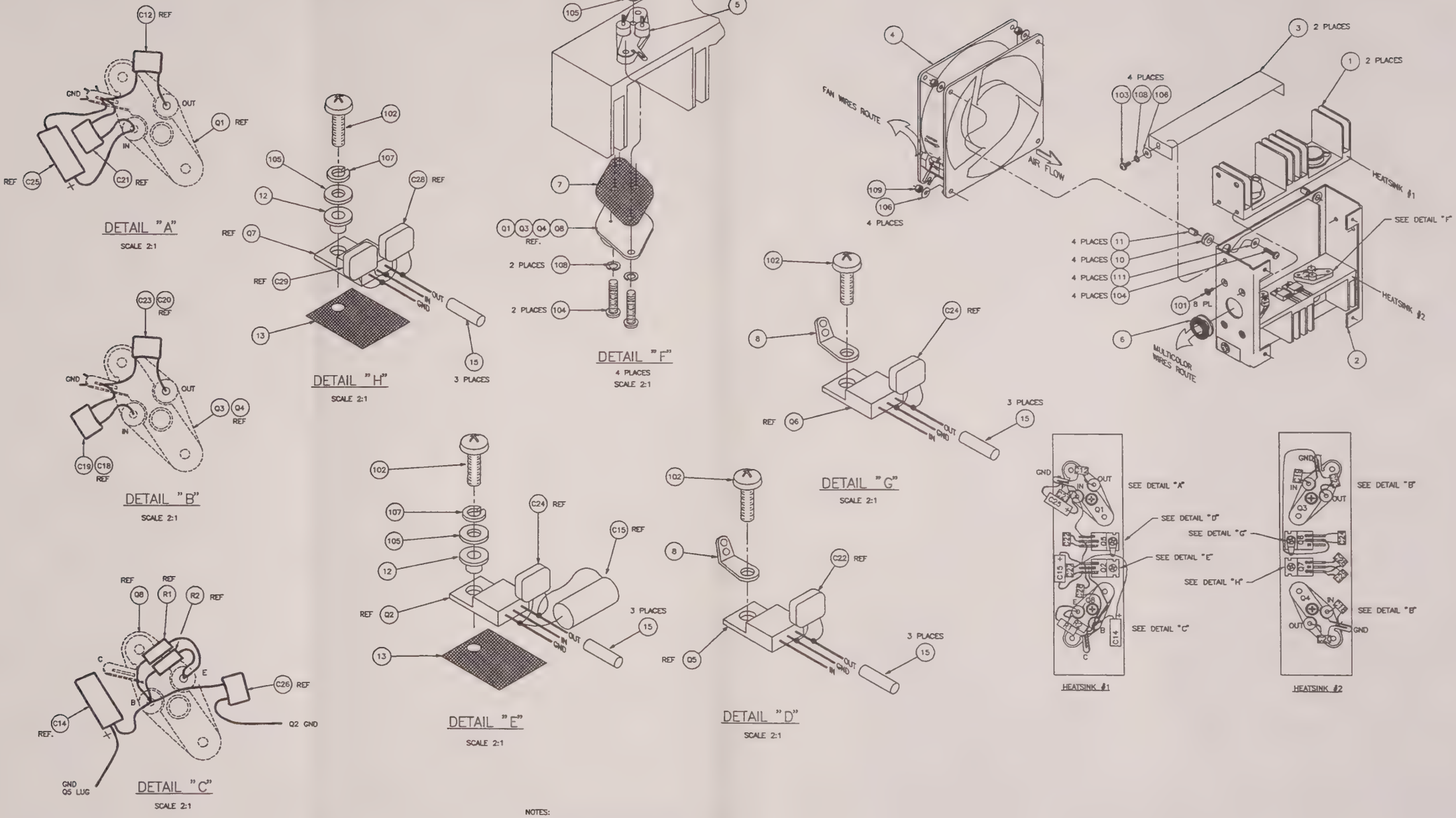




Computer Chassis Assy

DWG# 310BM16501 Rev D

Sheet 2 of 2



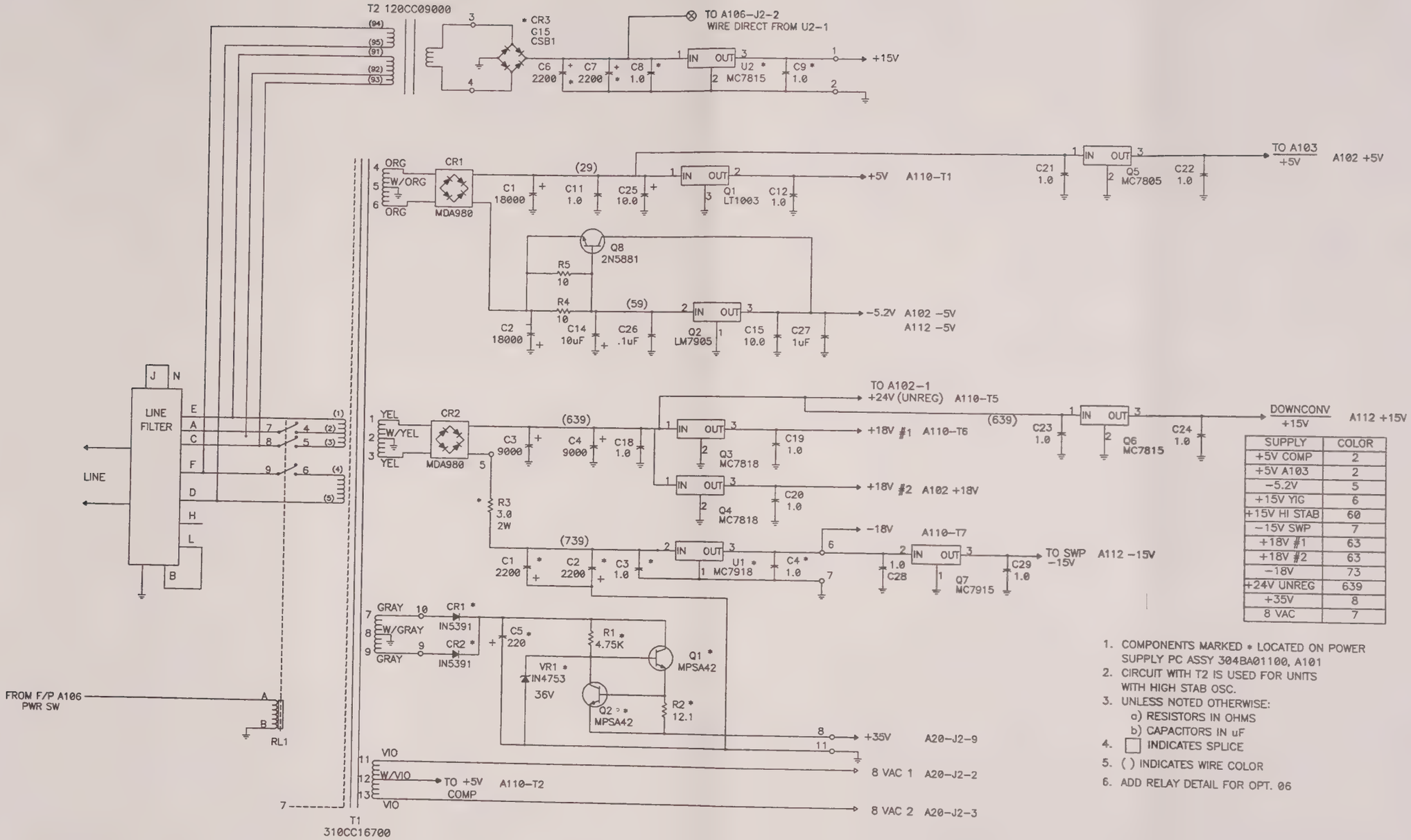
NOTES:

1. SEE SEPARATE PARTS LIST NUMBER 304DA14000.
2. SLEEVE WHERE NECESSARY, USING (14), NOT SHOWN.
3. CABLE TIE AS REQUIRED USING (16), NOT SHOWN.

Heatsink Assy

DWG# 310BM14000 Rev A

Sheet 1 of 1



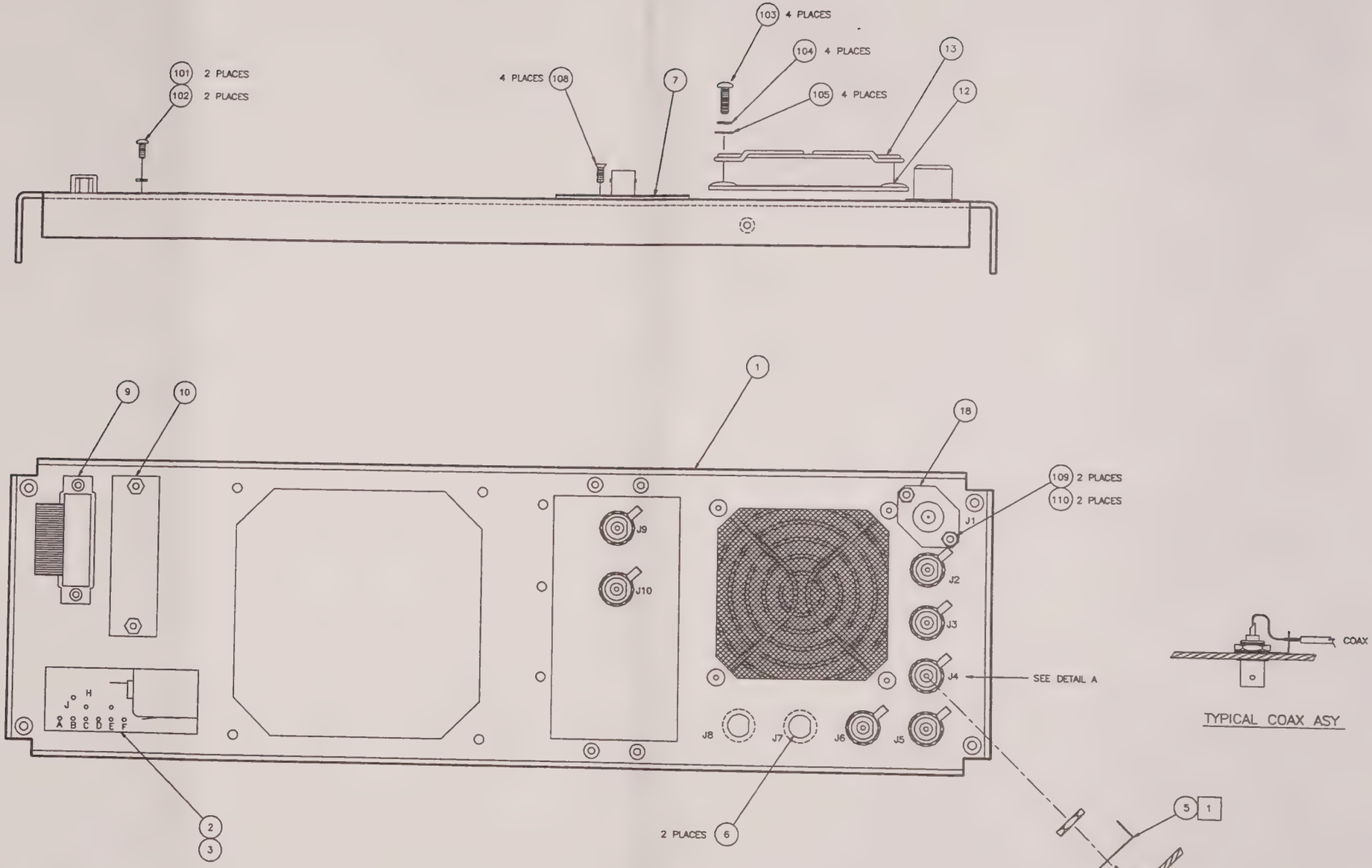
SUPPLY	COLOR
+5V COMP	2
+5V A103	2
-5.2V	5
+15V YIG	6
+15V HI STAB	60
-15V SWP	7
+18V #1	63
+18V #2	63
-18V	73
+24V UNREG	639
+35V	8
8 VAC	7

1. COMPONENTS MARKED * LOCATED ON POWER SUPPLY PC ASSY 304BA01100, A101
2. CIRCUIT WITH T2 IS USED FOR UNITS WITH HIGH STAB OSC.
3. UNLESS NOTED OTHERWISE:
   a) RESISTORS IN OHMS
   b) CAPACITORS IN uF
4. ☐ INDICATES SPLICE
5. ( ) INDICATES WIRE COLOR
6. ADD RELAY DETAIL FOR OPT. 06

Power Supply Assy

DWG# 310BM14100 Rev A

Sheet 1 of 1



NOTES: UNLESS OTHERWISE SPECIFIED

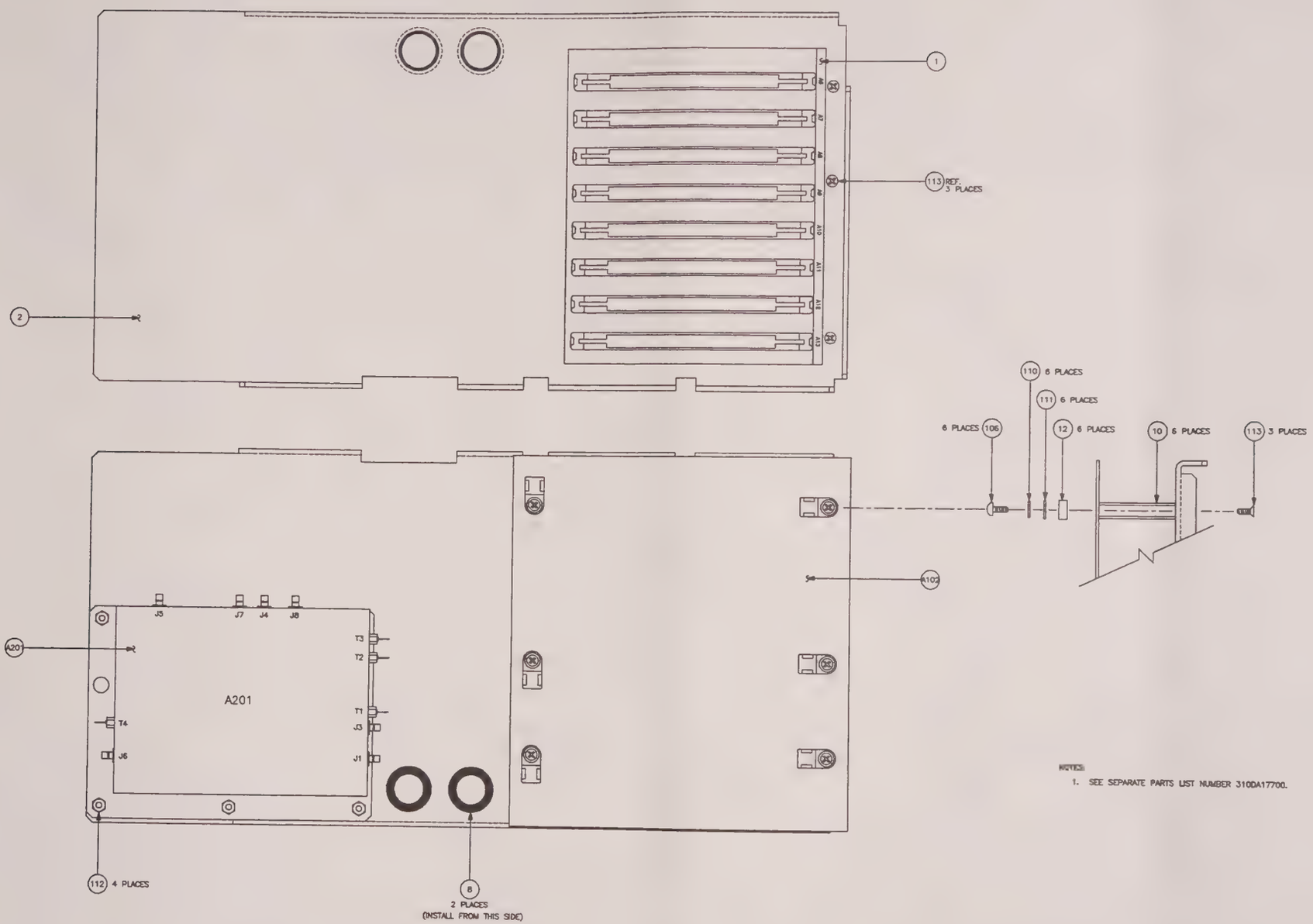
1. BEND SOLDER LUG APPROXIMATELY 90° AS SHOWN.
2. SEE SEPARATE PARTS LIST NUMBER 310DA10800.

Rear Panel Assy

DWG# 310BM10800 Rev B

Sheet 1 of 1

7-12

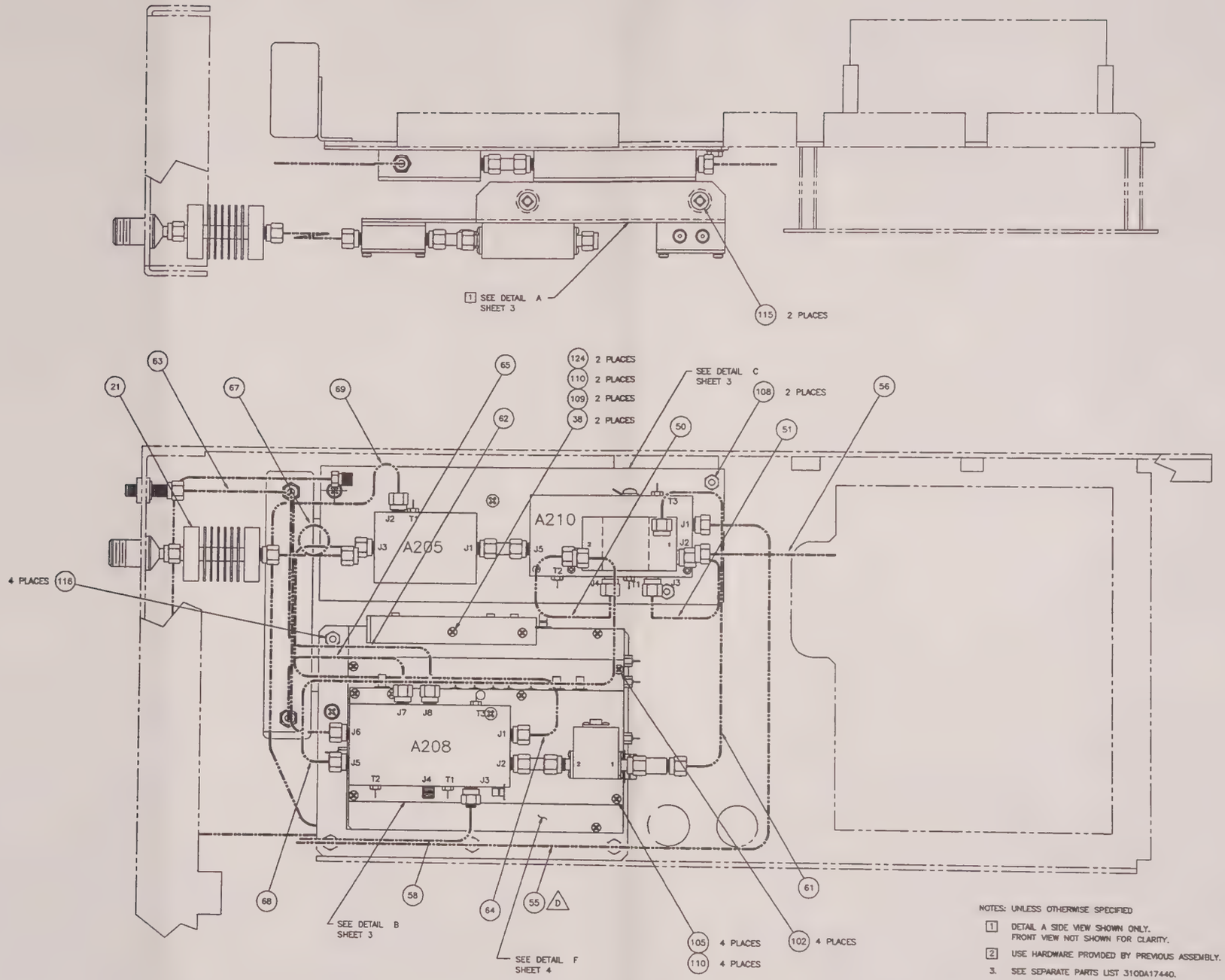


NOTES:

1. SEE SEPARATE PARTS LIST NUMBER 310DA17700.

RF Deck Assy

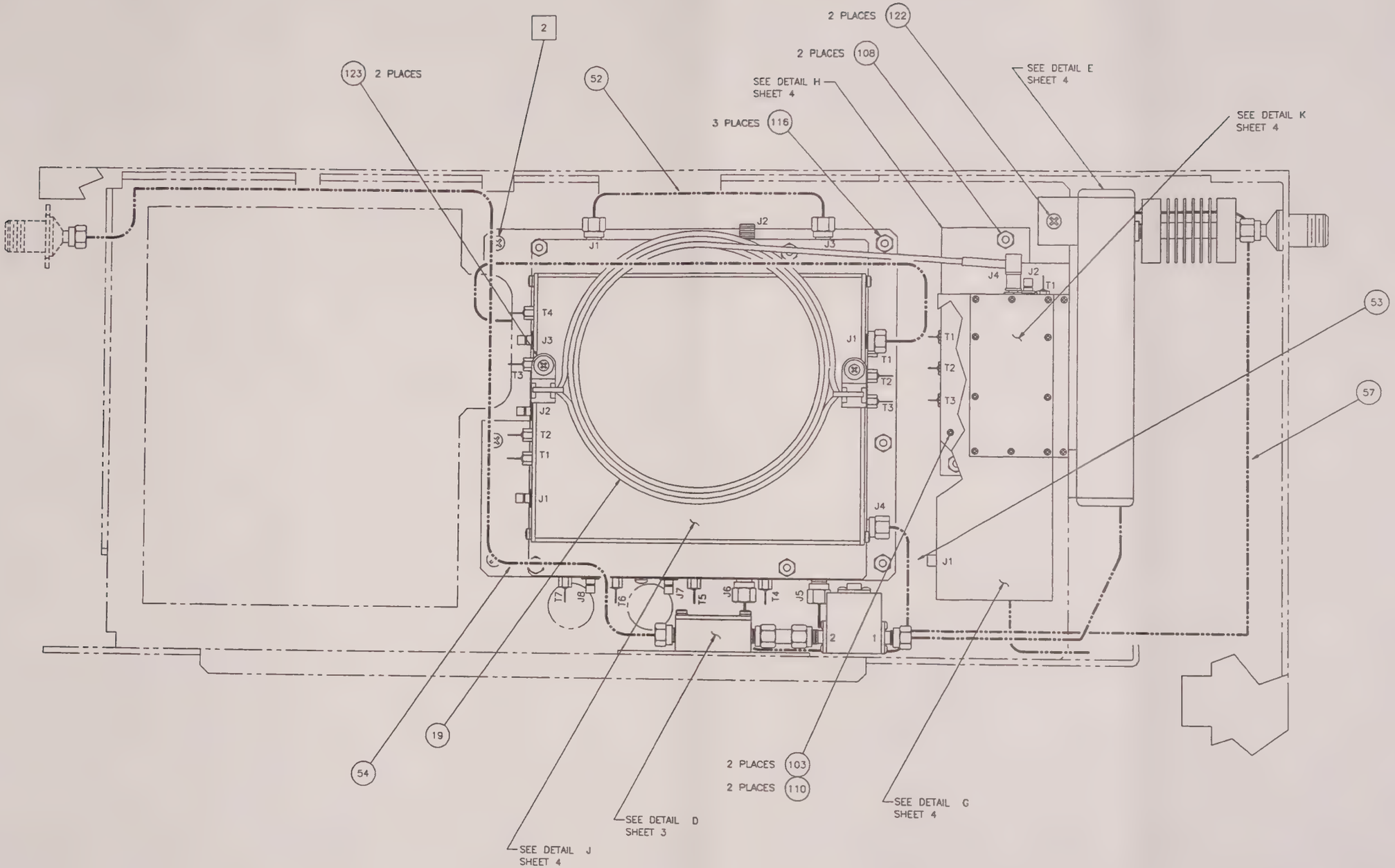
DWG# 310BM17700 Rev C


1 SEE DETAIL A SHEET 3
115 2 PLACES
124 2 PLACES
110 2 PLACES
109 2 PLACES
38 2 PLACES
SEE DETAIL C SHEET 3
108 2 PLACES
A210
A205
A208
4 PLACES 116
SEE DETAIL B SHEET 3
SEE DETAIL F SHEET 4
105 4 PLACES
110 4 PLACES
102 4 PLACES
NOTES: UNLESS OTHERWISE SPECIFIED
1 DETAIL A SIDE VIEW SHOWN ONLY. FRONT VIEW NOT SHOWN FOR CLARITY.
2 USE HARDWARE PROVIDED BY PREVIOUS ASSEMBLY.
3. SEE SEPARATE PARTS LIST 310DA17440.
4. ITEMS 2 AND 3 NOT SHOWN.

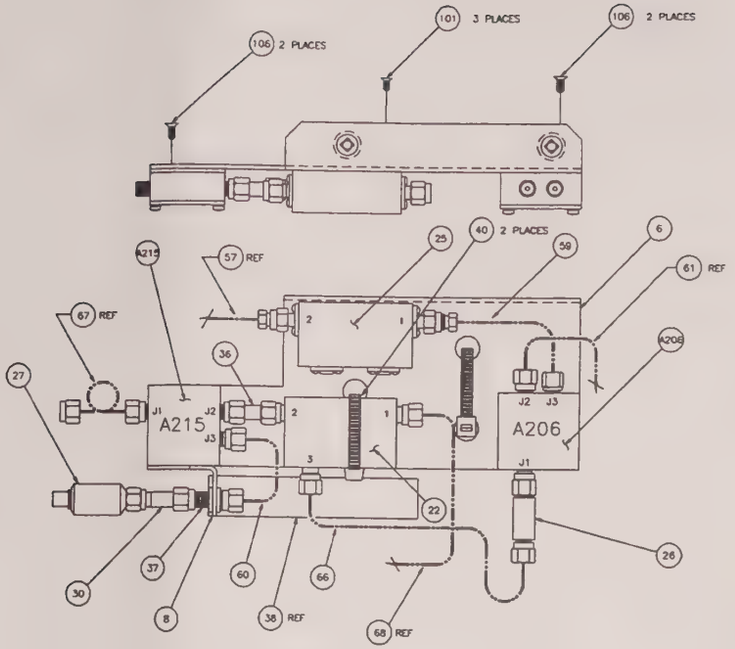
Freq. 9.0-9.5 WR-109 Assy

DWG# 310BM17440 Rev D

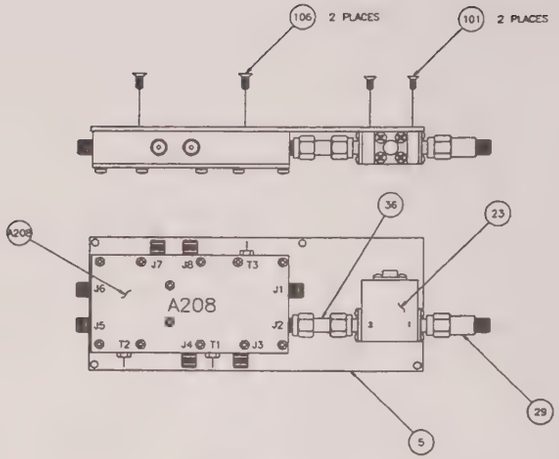
Sheet 1 of 4


2
123 2 PLACES
52
2 PLACES 122
2 PLACES 108
SEE DETAIL E
SHEET 4
SEE DETAIL H
SHEET 4
3 PLACES 116
SEE DETAIL K
SHEET 4
J1
J2
J3
J4
T1
T2
T3
T4
53
57
19
54
2 PLACES 103
2 PLACES 110
SEE DETAIL D
SHEET 3
SEE DETAIL J
SHEET 4
SEE DETAIL G
SHEET 4

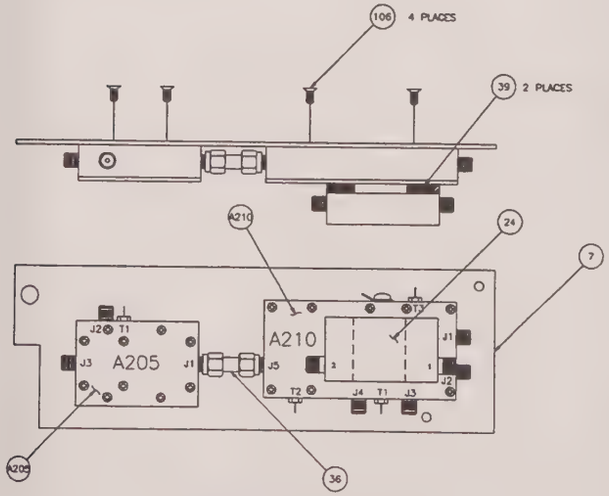
REAR VIEW



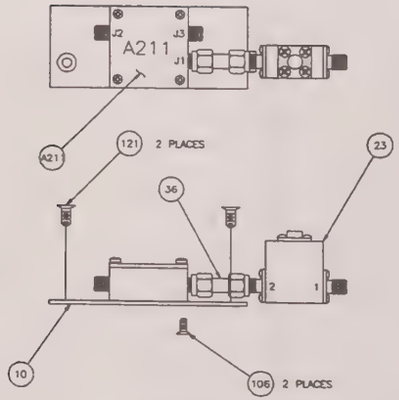
DETAIL A



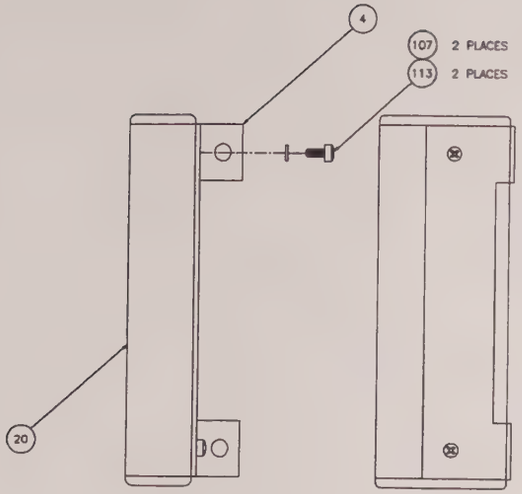
DETAIL B



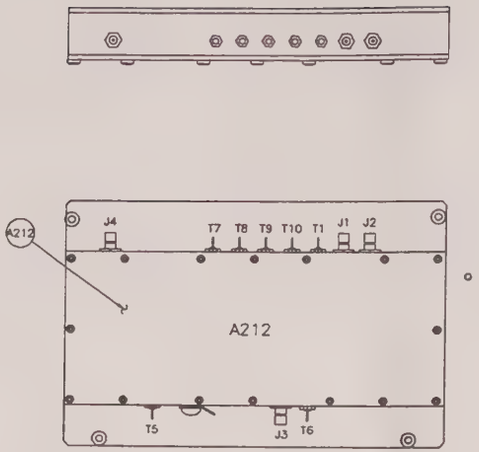
DETAIL C



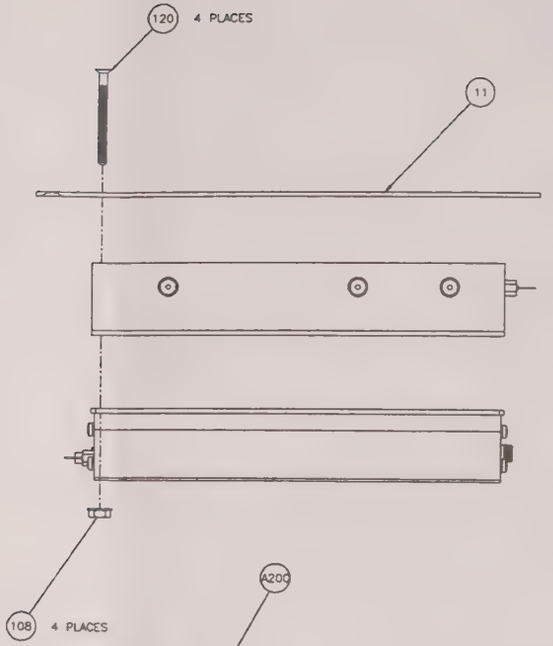
DETAIL D

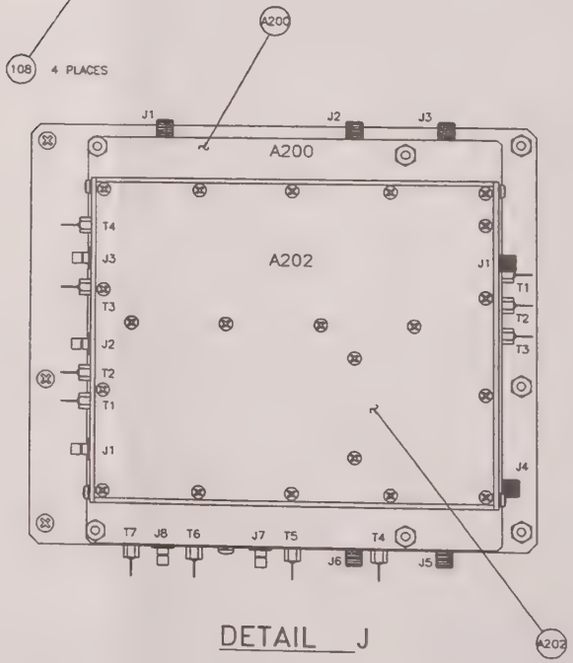


DETAIL E

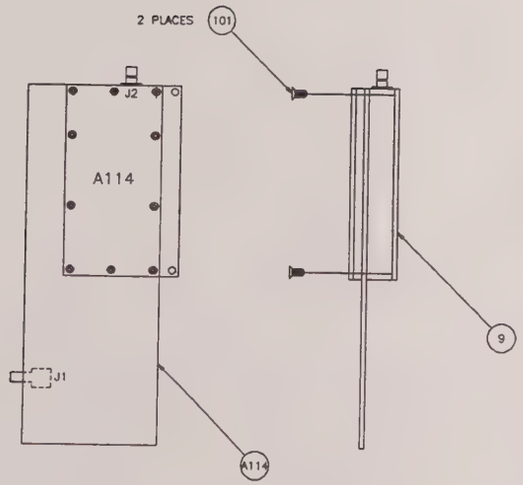


DETAIL F

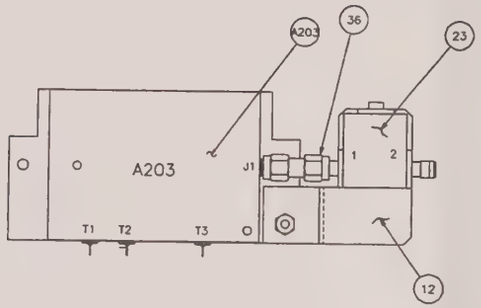


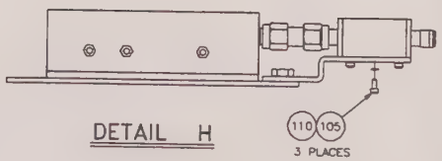


DETAIL J

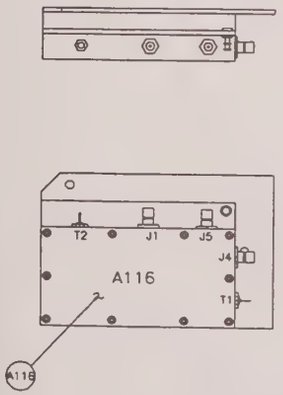


DETAIL G





DETAIL H

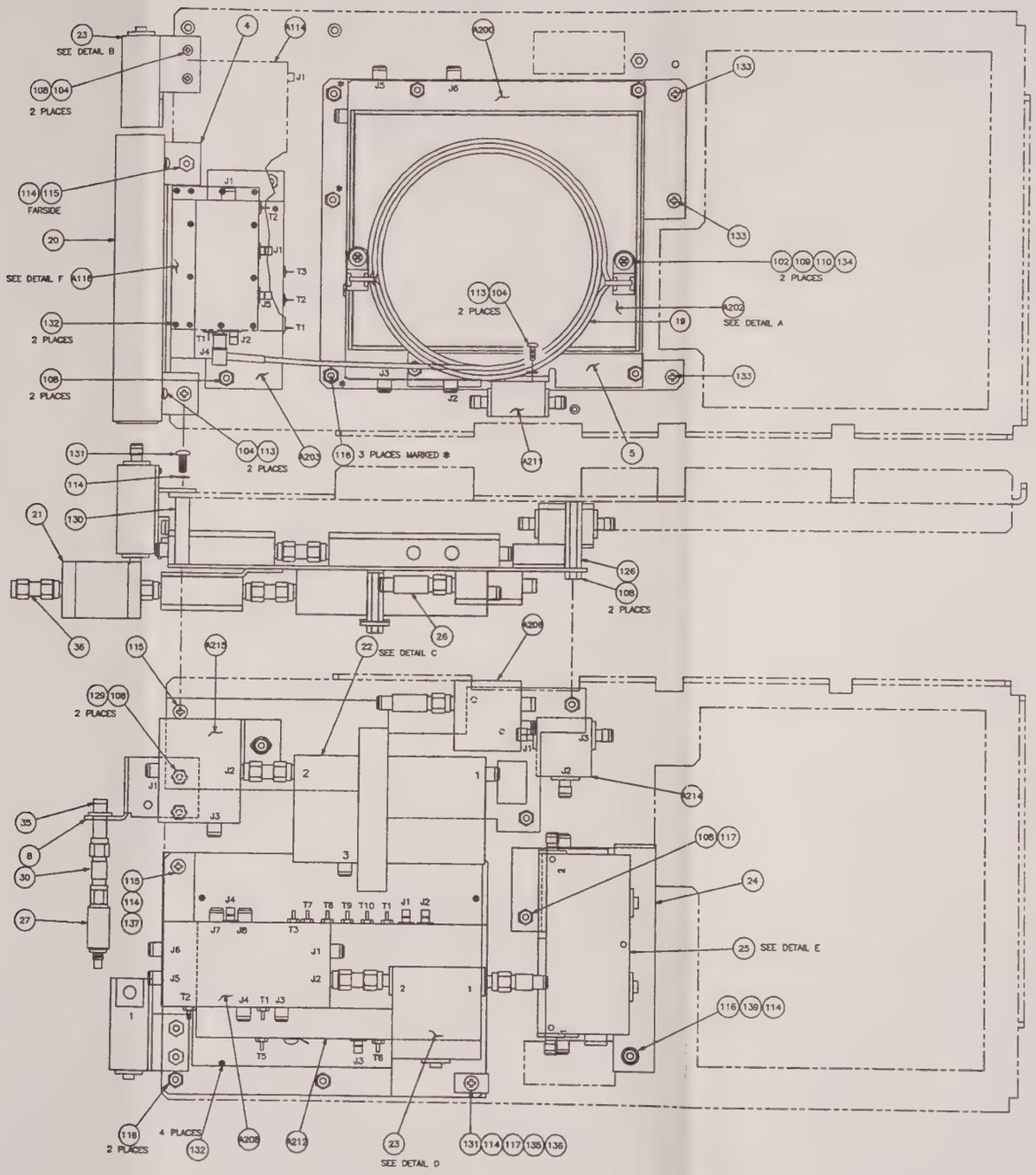


DETAIL K

Freq. 9.0-9.5 WR-109 Assy

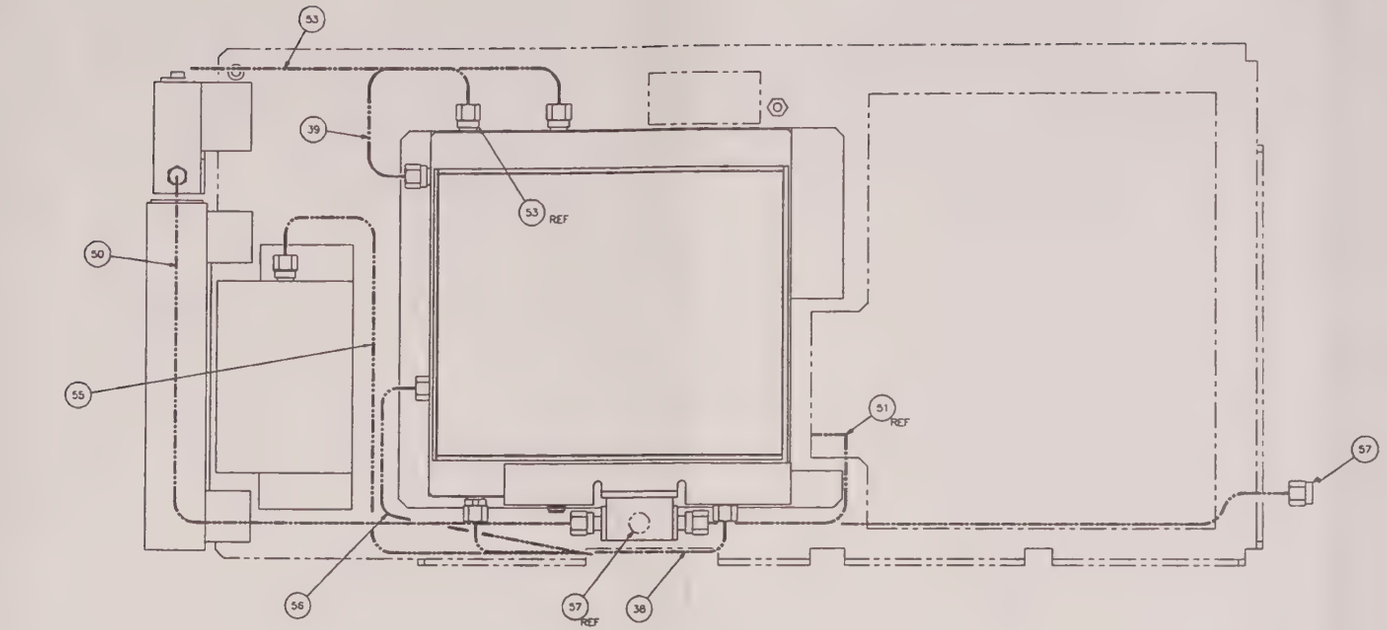
DWG# 310BM17440 Rev D

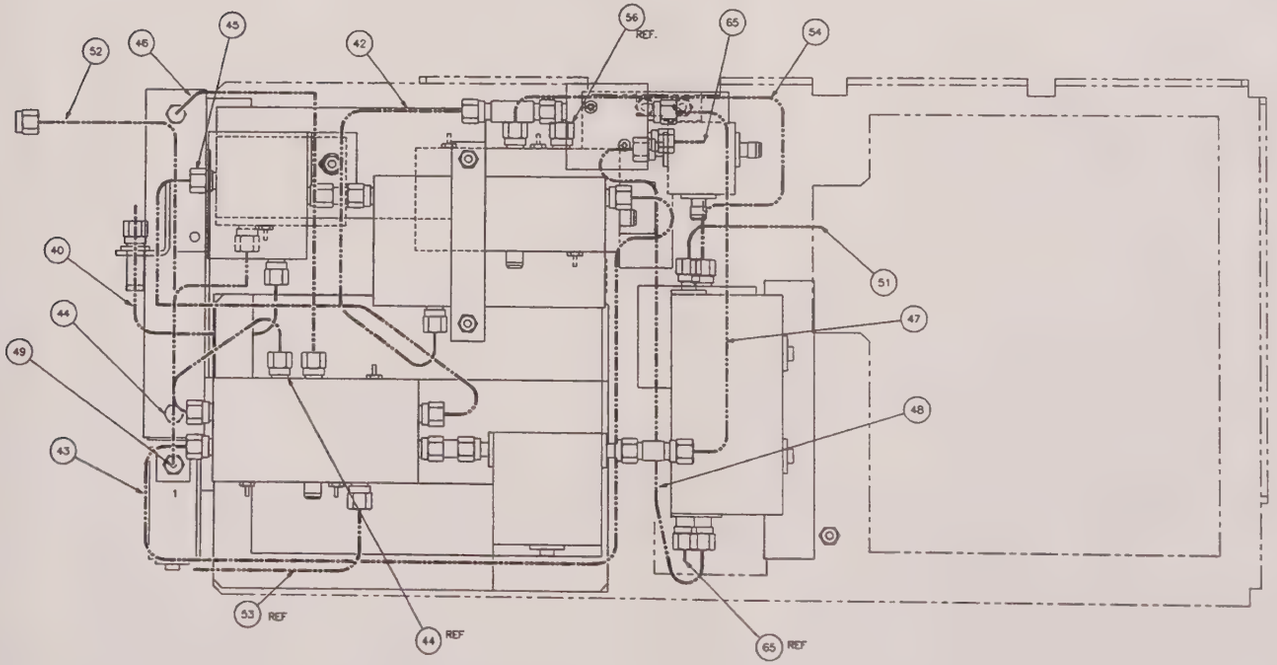
Sheet 4 of 4



NOTES:

1. NOT SHOWN ITEM 2 & 3.
2. INSTALL SEMI-RIGID AT THIS STAGE OF ASY.
3. SEE SEPARATE PARTS LIST NUMBER 310DA17420.

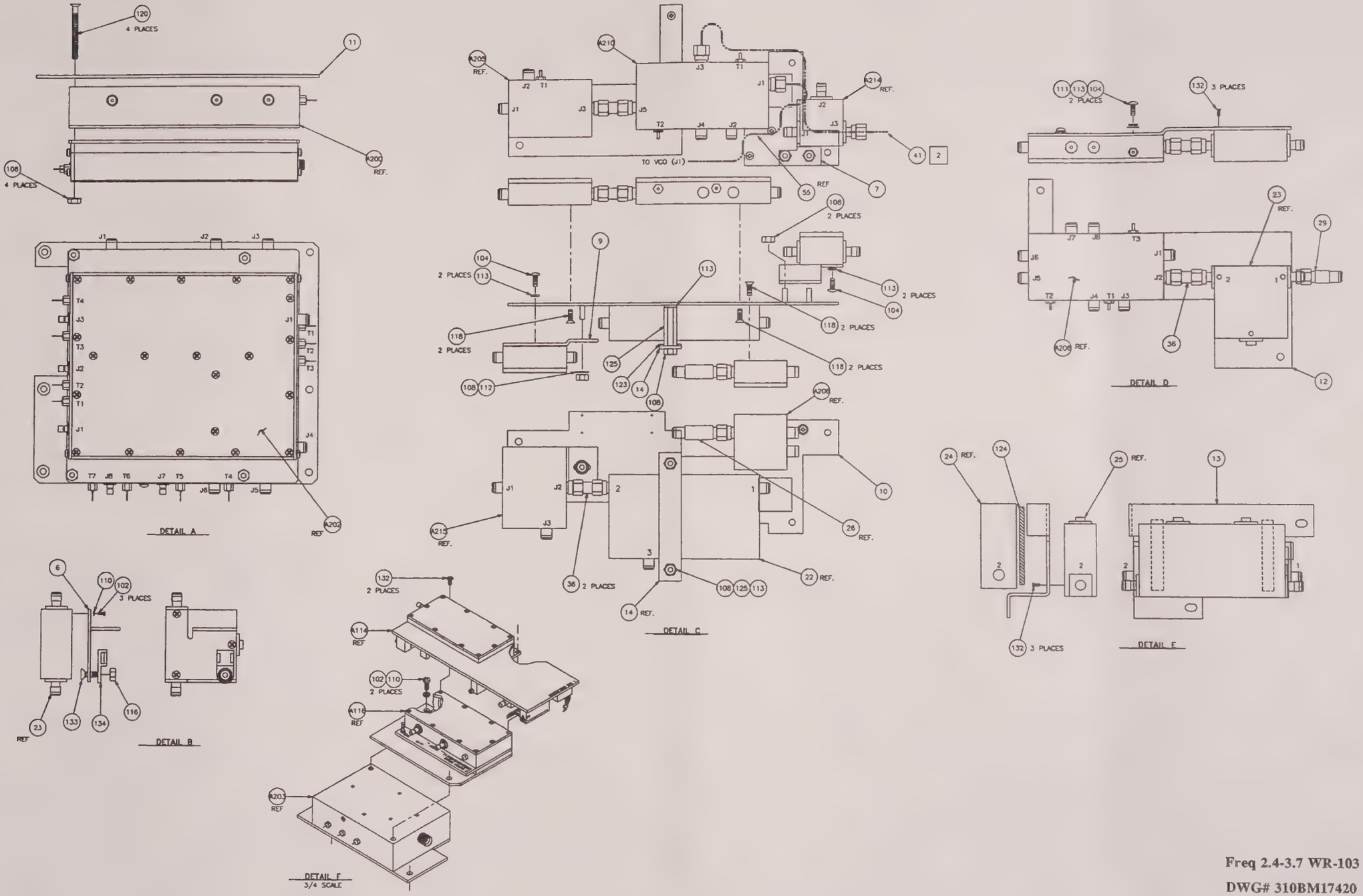




Freq 2.4-3.7 WR-103 Assy

DWG# 310BM17420 Rev 11

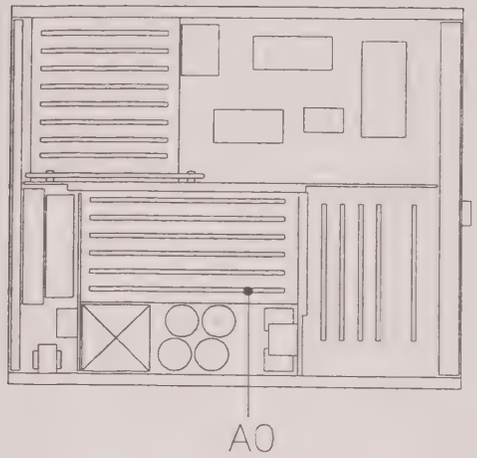
Sheet 2 of 3



Freq 2.4-3.7 WR-103 Assy

DWG# 310BM17420 Rev 11

Sheet 3 of 3

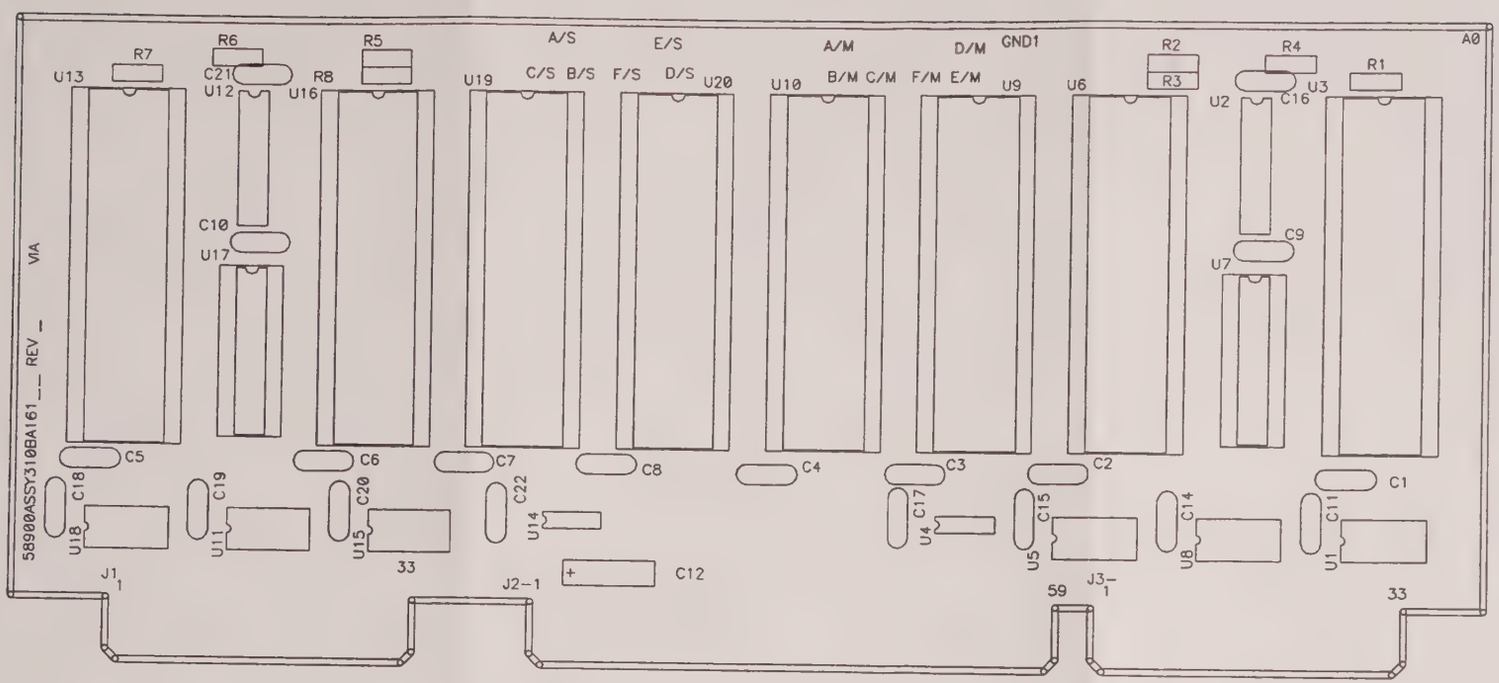


VIA (A0)

DWG# 310BM16100 Rev A

Sheet 1 of 4

7-A0-1

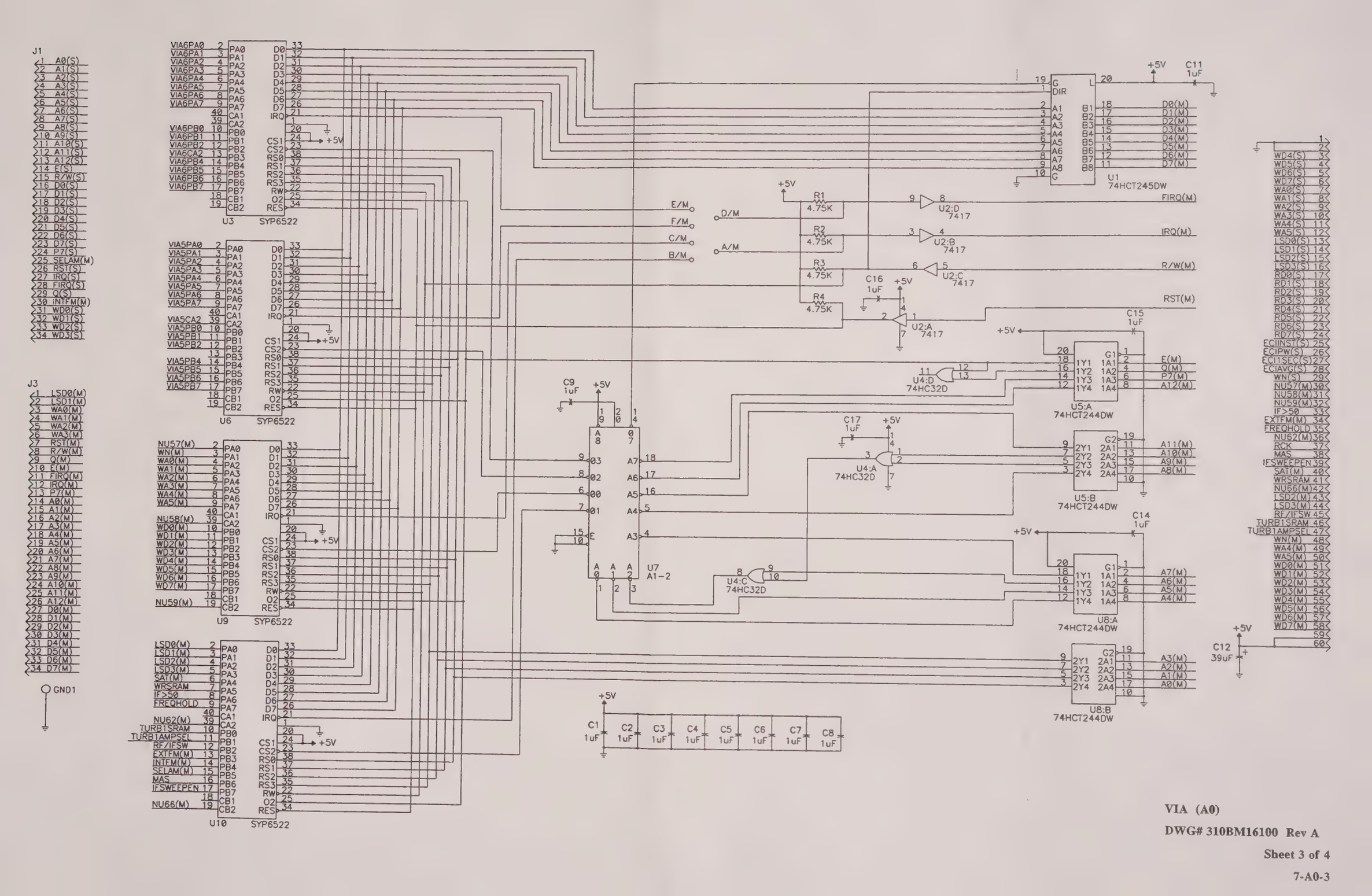


VIA -- PC ASSY A0

The VIA PCA provides the ability for the instrument computer to communicate with various circuits in the unit. The individual data and address lines are buffered to prevent loading of the system bus. Fuse-link PROM U5 and U17 decode the address lines to provide 'chip selects' for the I/O devices.

The VIA PCA has two groups of peripheral adapters which are controlled by the master CPU and slave CPU independently. U3 and U6 serve as internal bus adapters for the master side and U13 and U16 serve as internal bus adapters for the slave side. They are connected to each other through their "ports" and control all of the data communication between the two sides.

U9 and U10 provide four "ports" of eight bits each for the master CPU to communicate and control with the peripheral devices. U19 and U20 provide four "ports" for the slave CPU.

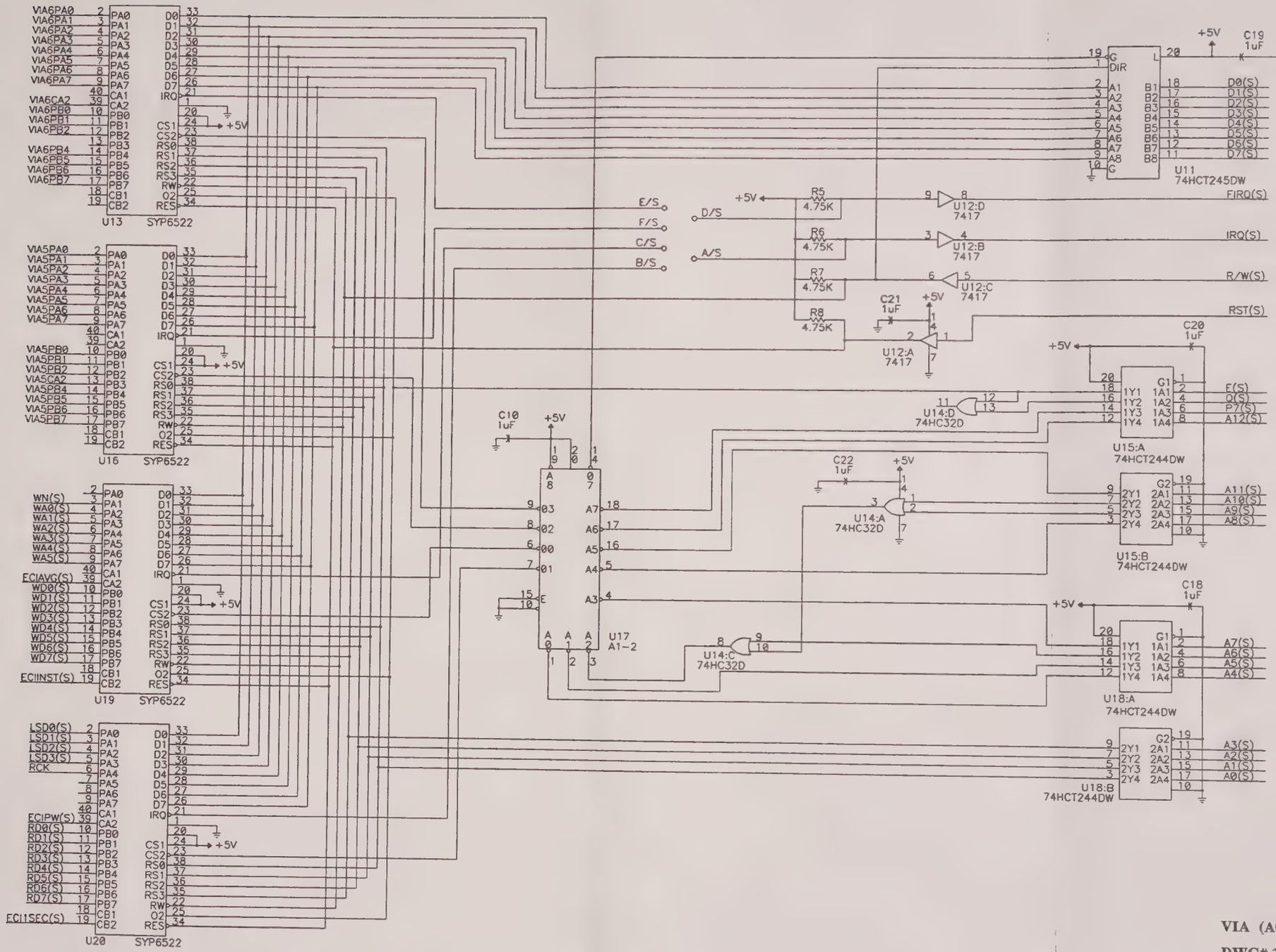


VIA (A0)

DWG# 310BM16100 Rev A

Sheet 3 of 4

7-A0-3

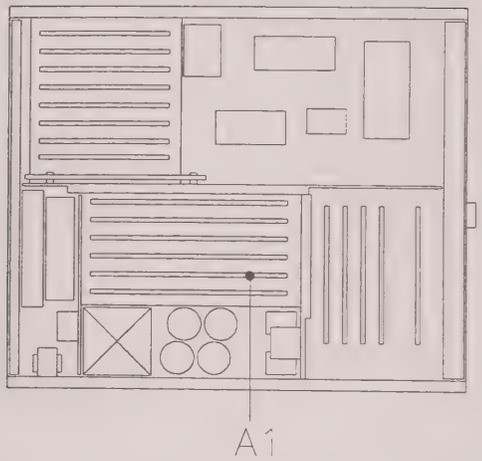


VIA (A0)

DWG# 310BM16100 Rev A

Sheet 4 of 4

7-A0-4

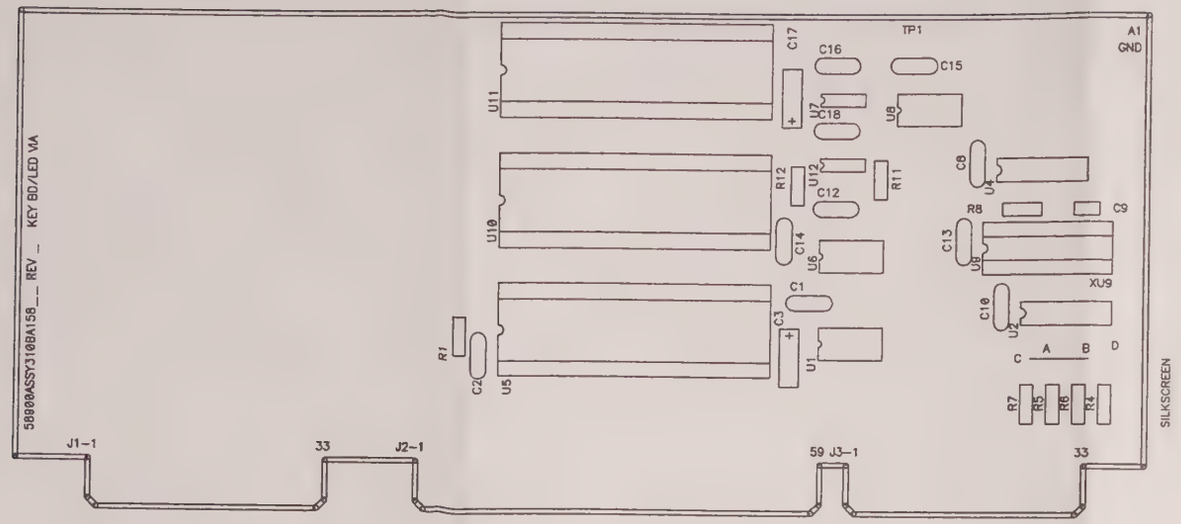


Keyboard/VIA (A1)

DWG# 310BM15800 Rev A

Sheet 1 of 3

7-A1-1



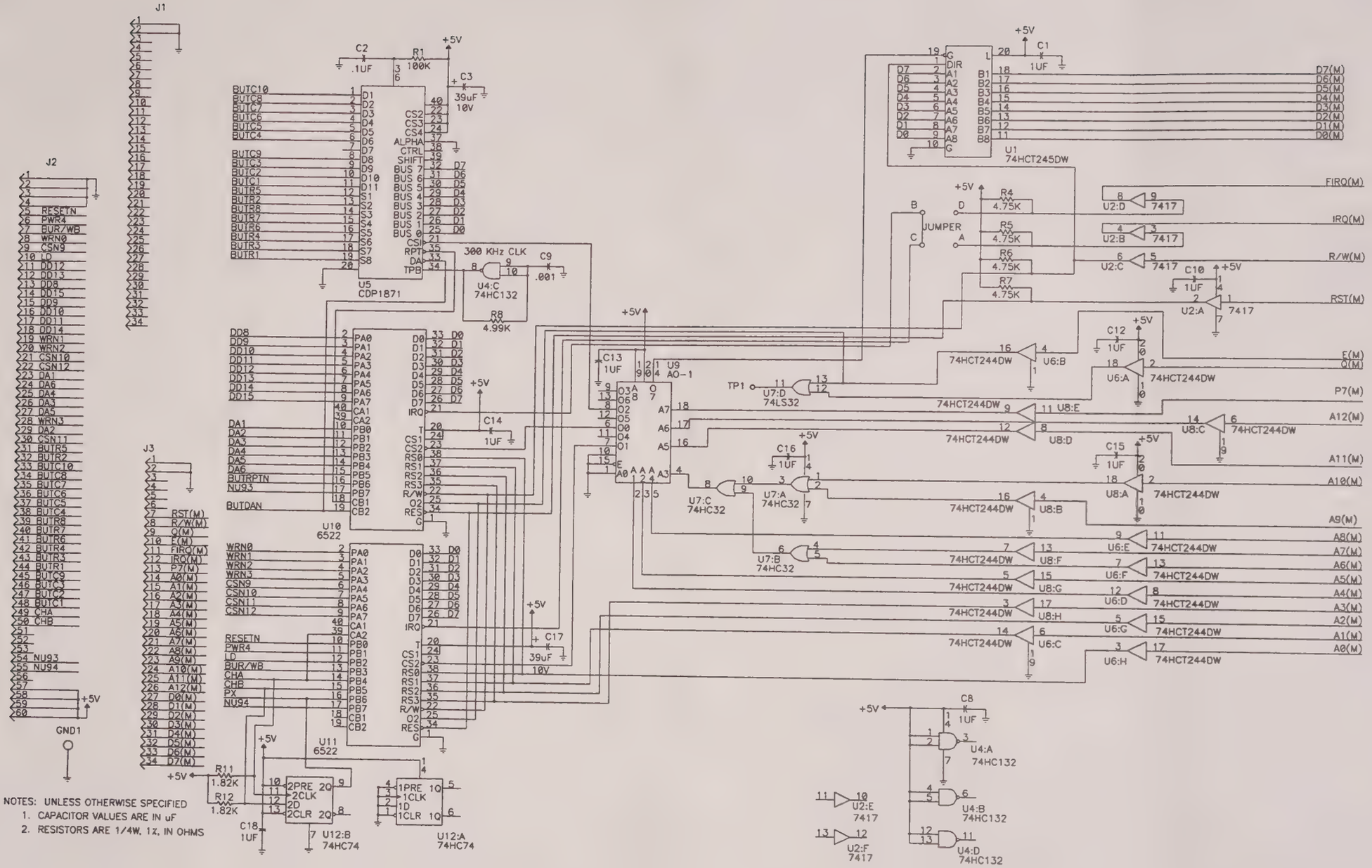
KEYBOARD/LED VIA -- PC ASSY A1

The Keyboard/LED VIA PCA provides an interface between the instrument computer and many of the front panel functions. Individual data and address lines are buffered to reduce loading on the system bus. Fuse-link PROM U7 decodes the address lines to provide 'chip selects' for the I/O devices.

A dedicated interface, U5, is used to 'read' the output of the various buttons on the panel. The buttons are arranged in a 'row/column' matrix which is constantly polled by U5. U4 provides a 300 kHz clock for U5.

Peripheral Interface Adapters U10 and U11 provide a variety of data and address lines for the balance of the front panel indicators.

Dual flip-flop U12 is used to translate the output from the rotary encoder on the front panel. It determines the direction of rotation in conjunction with the inputs to U11.



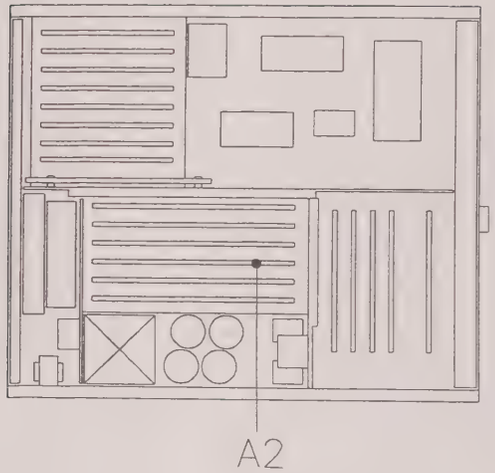
NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF
2. RESISTORS ARE 1/4W, 1%, IN OHMS

Keyboard/VIA (A1)

DWG# 310BM15800 Rev A

Sheet 3 of 3

7-A1-3

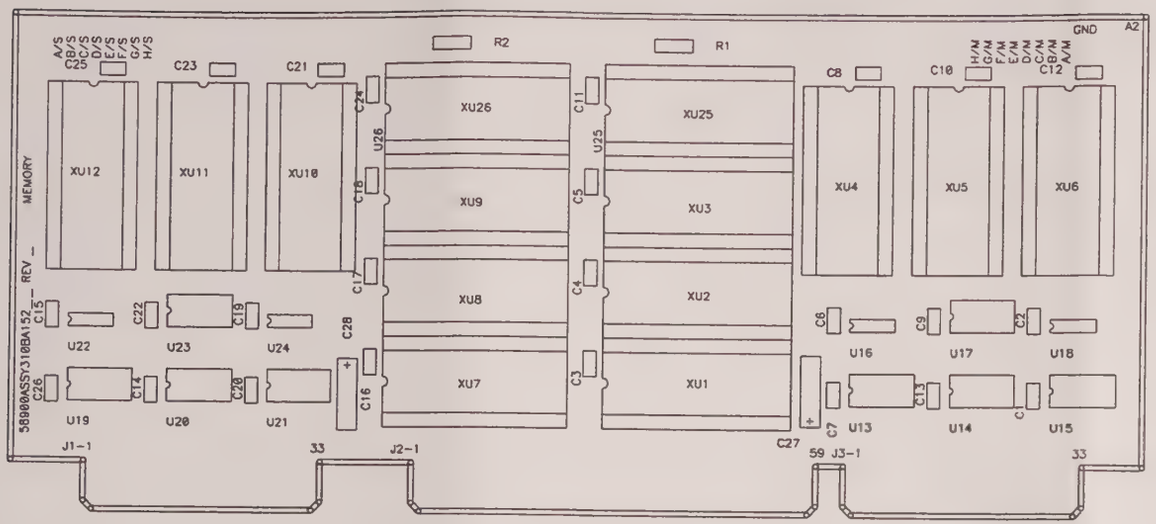


Memory (A2)

DWG# 310BM15200 Rev B

Sheet 1 of 5

7-A2-1



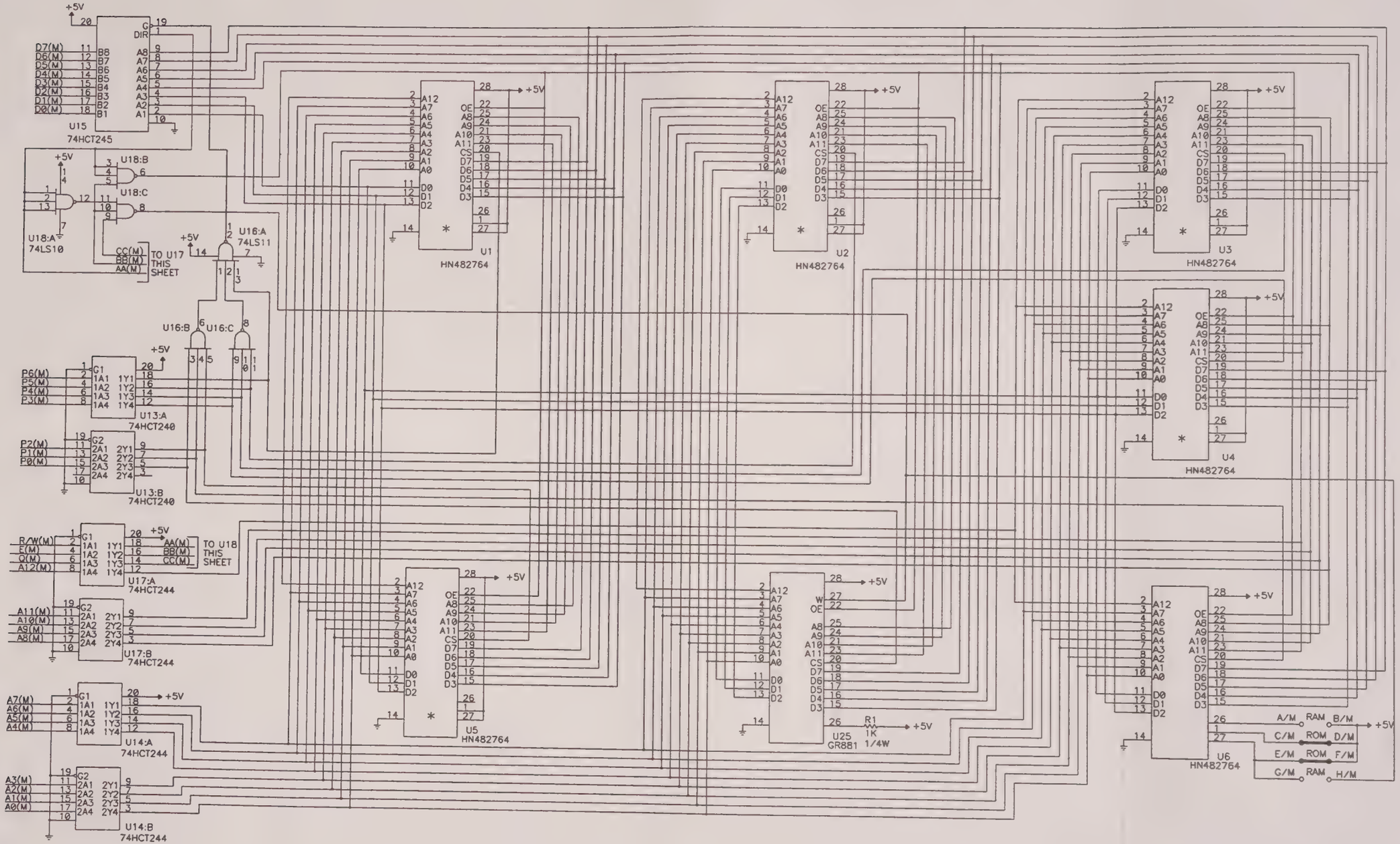
MEMORY -- PC ASSY A2

The memory board is divided into two separate circuits which serve the master side and the slave side of the CPU. The master side memory is shown on sheet 3; the slave side memory (sheet 4) is a duplicate of the master side. The following description of the master side also applies to the slave side, except that the component callouts have different numbers.

U1 through U6 are are PROMs; each of them has a capacity of 8K bytes. The PROMs hold the instrument's operational software. The amount of memory actually installed is variable, depending upon the requirements of the instrument. A non-volatile 8K RAM (U25) is also installed. The remaining 8K of the master processor's memory addressing capacity is taken up by the "reset" PROM on the CPU board, and by input/output ports.

A bi-directional buffer (U15) connects the 8-bit CPU data bus with the memory devices on this board. The CPU's address bus and some control lines are buffered by U13, U17, and U14. Logic gates U18 and U16 decode some of these inputs in order to derive control signals for the memories and the bi-directional buffer. The CPU uses page lines P0 through P6 to select individual memory chips.

The address and data buses of the memory ICs are all connected in parallel; this is possible because the ICs have tri-state outputs (the outputs enter a high-impedance state when the chip is de-selected).

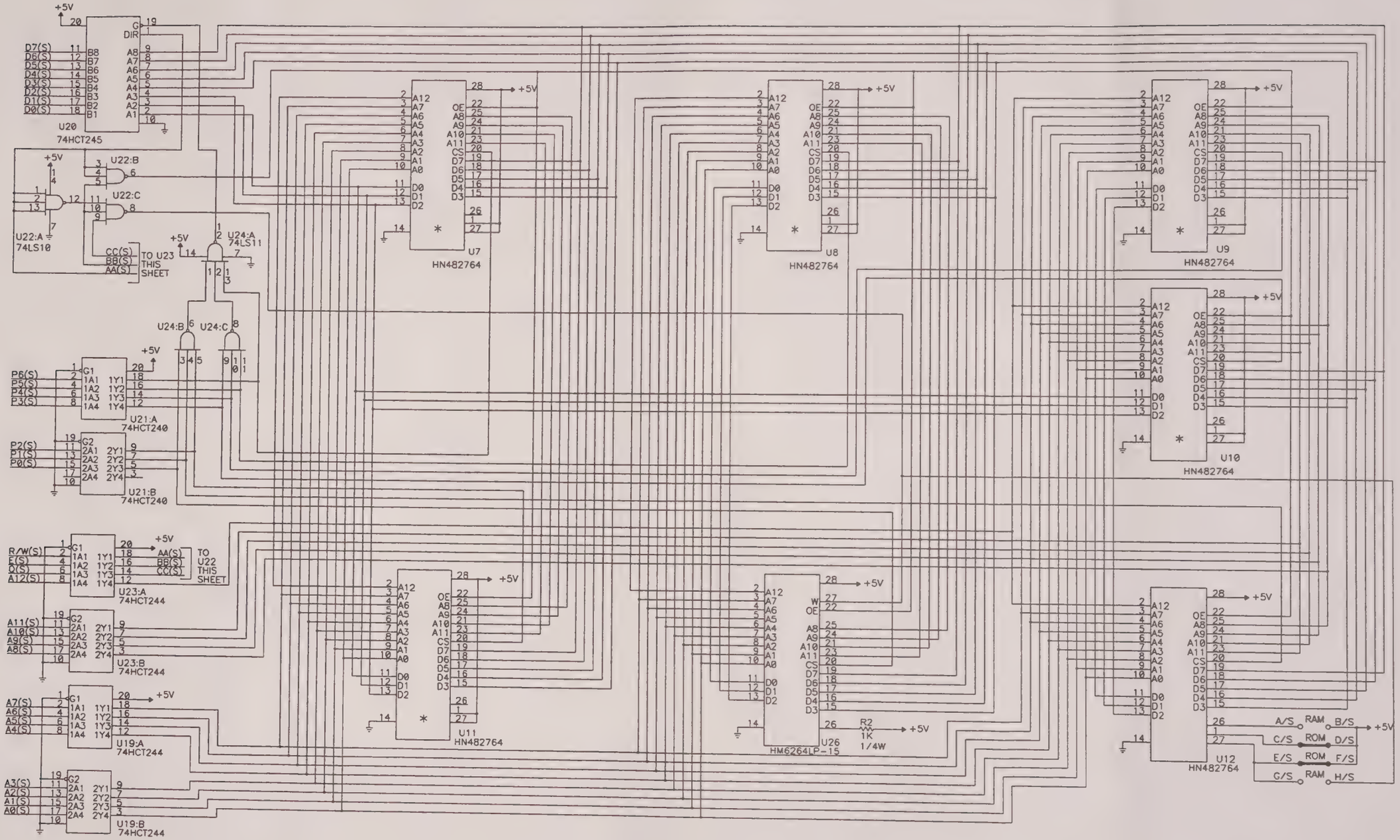


Memory (A2)

DWG# 310BM15200 Rev B

Sheet 3 of 5

7-A2-3

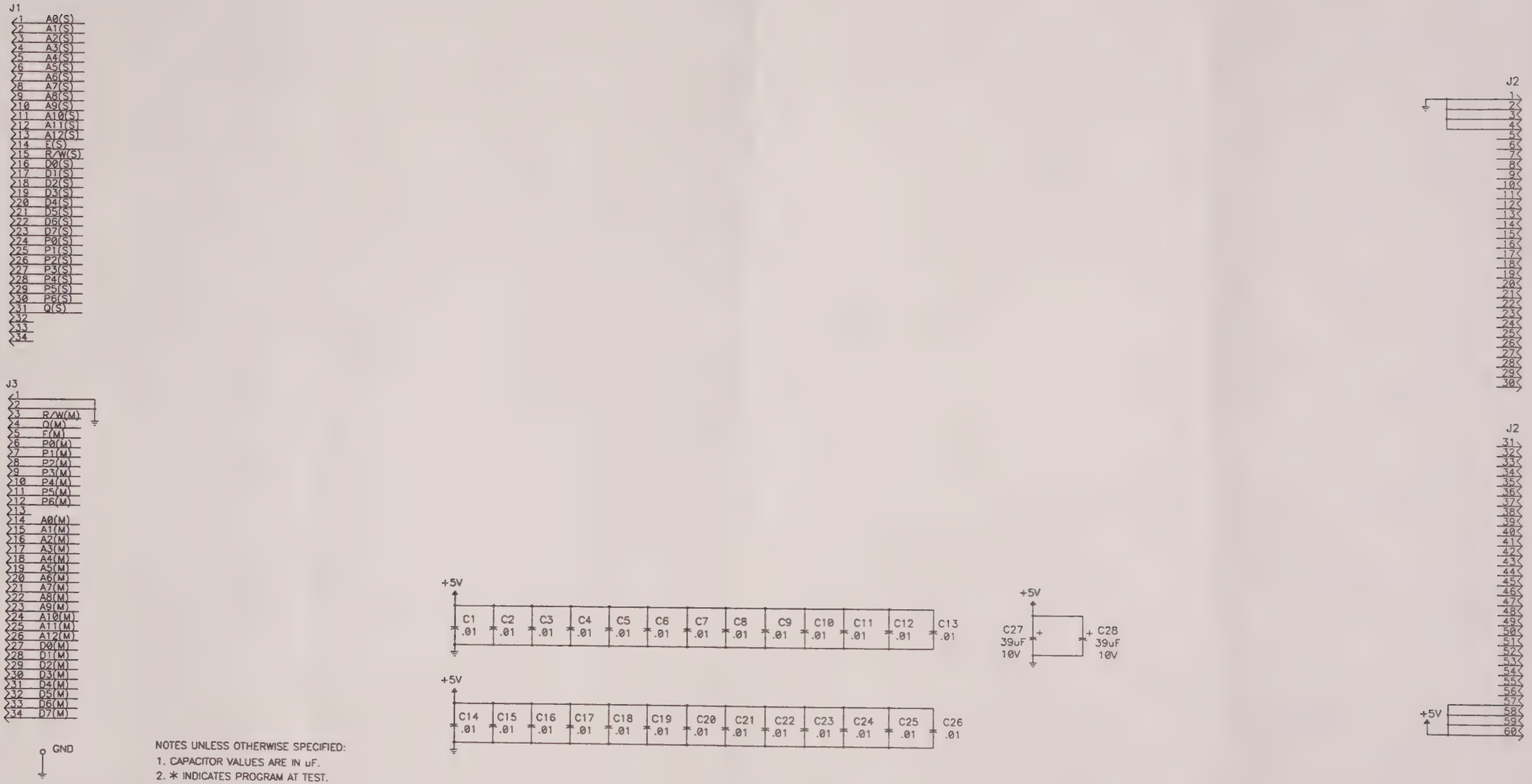


Memory (A2)

DWG# 310BM15200 Rev B

Sheet 4 of 5

7-A2-4



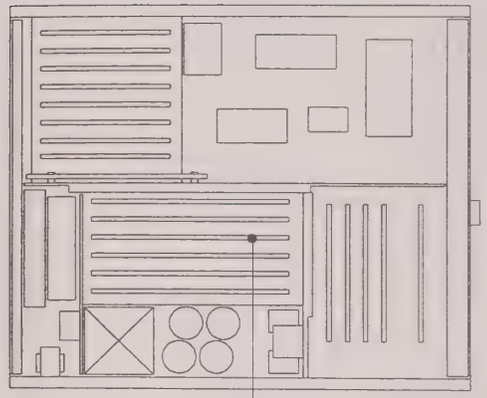
NOTES UNLESS OTHERWISE SPECIFIED:
1. CAPACITOR VALUES ARE IN uF.
2. * INDICATES PROGRAM AT TEST.

Memory (A2)

DWG# 310BM15200 Rev B

Sheet 5 of 5

7-A2-5

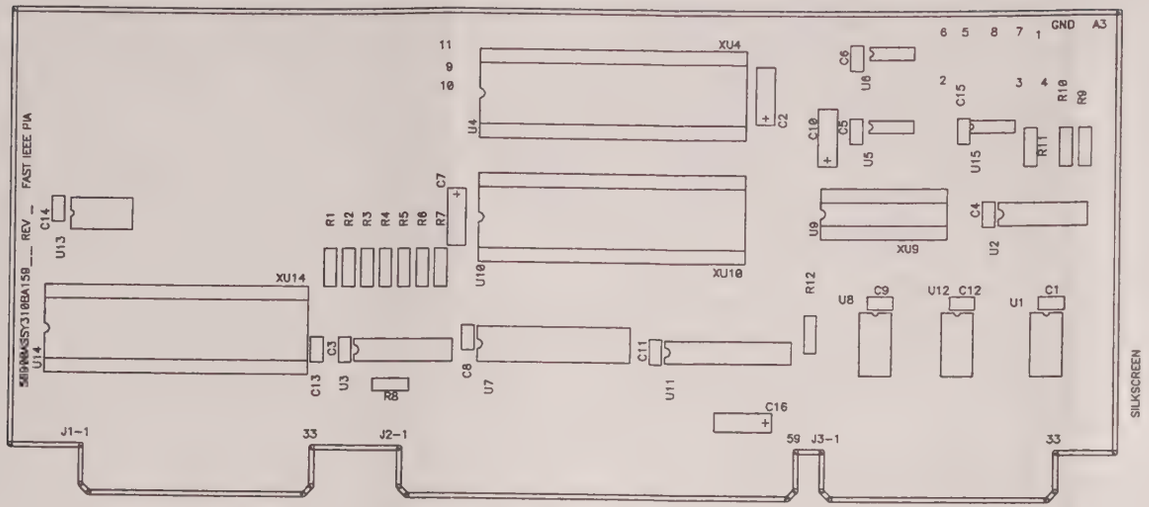


Fast IEEE (A3)

DWG# 310BM15900 Rev A

Sheet 1 of 3

7-A3-1



FAST IEEE -- PC ASSY A3

GENERAL

This portion of the system computer provides communication between the microprocessor and any external controller using the IEEE-488 general purpose interface bus (GPIB). The circuit board also houses a peripheral interface adapter (PIA) and a versatile interface adapter (VIA) which are used for a variety of instrument control functions.

COMPUTER BUS

A bidirectional buffer (U1) is used to interconnect the computer's 8-bit data bus with the PIA and GPIB devices. The computer's address bus and some control lines are buffered by U2, U8 and U12, and are decoded by a high speed bipolar PROM (U9), and by additional logic gates. The outputs of the decoder PROM are used to drive chip select lines on the input/output devices and GPIB devices and also to drive the data direction gate of the buffer (U1).

IEEE-488 INTERFACE

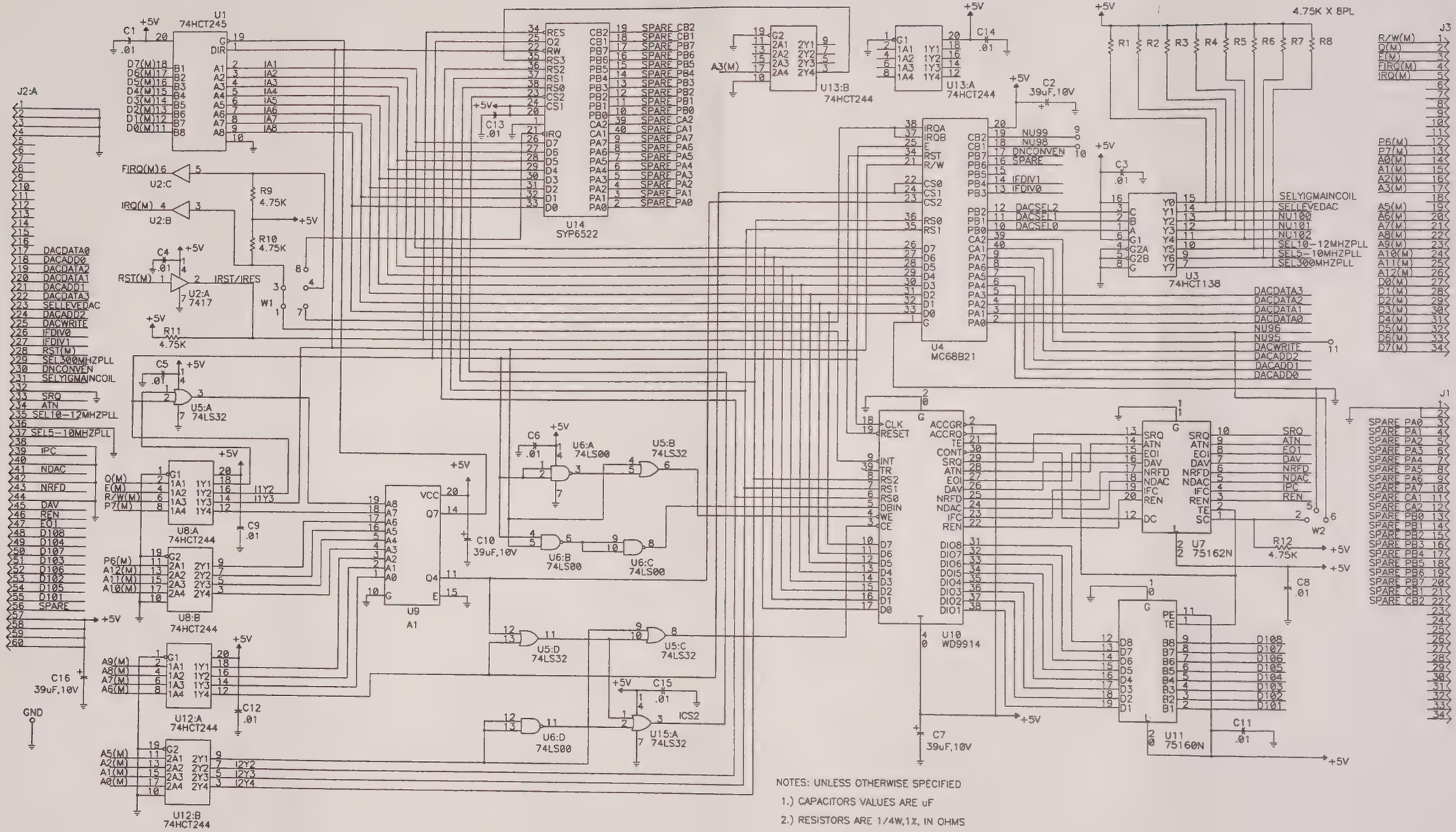
The GPIB adapter (U10) facilitates communication between the IEEE-488 interface bus and the system computer's data bus. It processes the general "interface" messages received from the controller, and transmits device-dependent messages (such as commands addressed specifically to this instrument) to the computer. The computer interprets these messages, using a vocabulary stored in ROM, and responds appropriately; the GPIB adapter transmits the computer's outgoing messages to the bus. The data and control lines between the GPIB adapter and the 24-pin connector on the rear panel are buffered by U7 and U11.

PERIPHERAL INTERFACE ADAPTER

The PIA (U4) is a programmable port through which information is transmitted between the computer's data bus and other devices. Three of its outputs are decoded by IC12 into eight control lines. The PIA is used for various instrument control functions, including the programming of digital to analog converters.

VERSATILE INTERFACE ADAPTER

The U14 VIA is a spare input/output device reserved for later use.

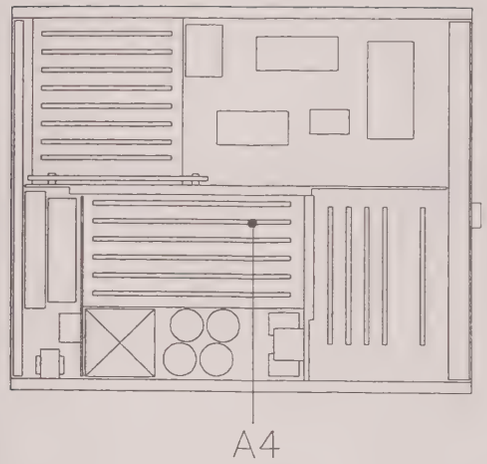


Fast IEEE (A3)

DWG# 310BM15900 Rev A

Sheet 3 of 3

7-A3-3

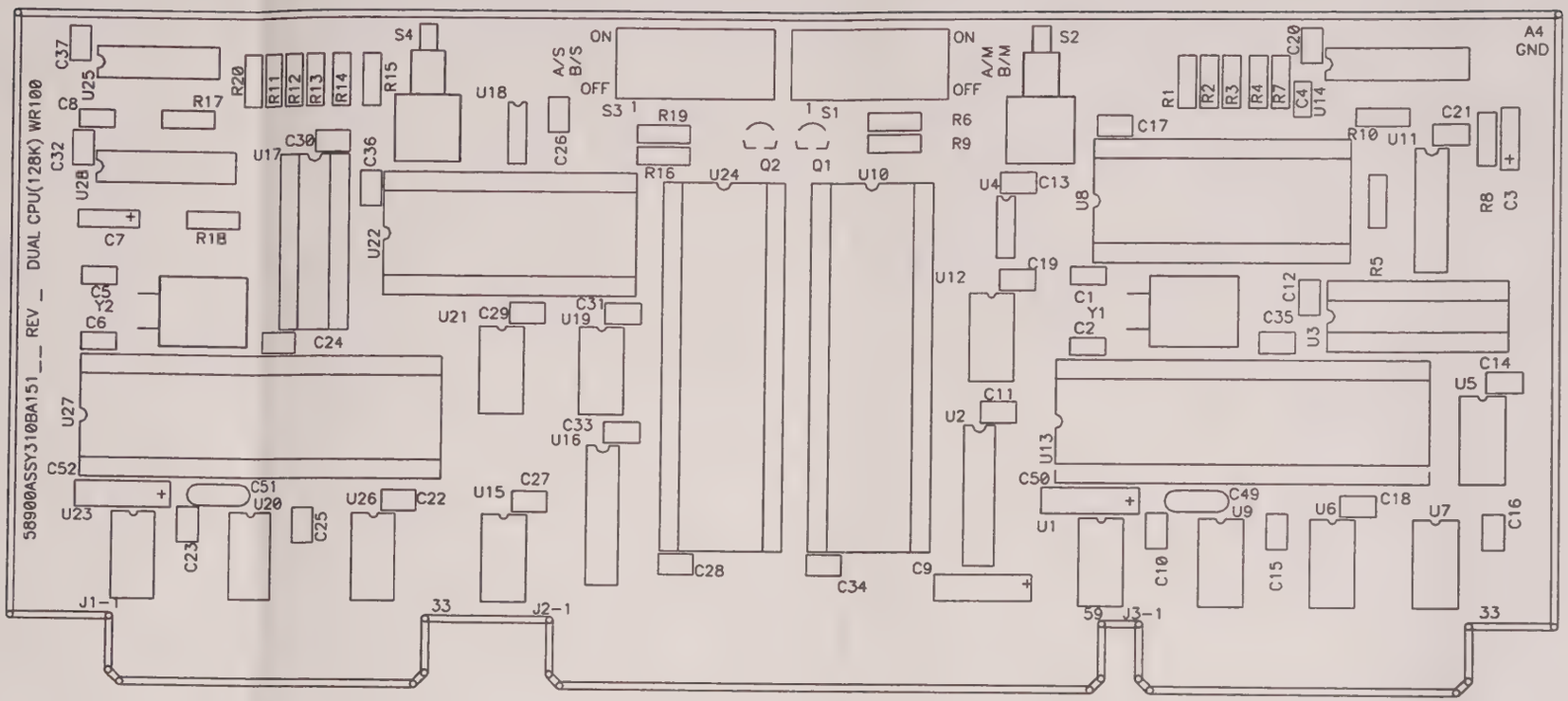


Dual Microprocessor CPU (A4)

DWG# 310BM15100 Rev B

Sheet 1 of 5

7-A4-1



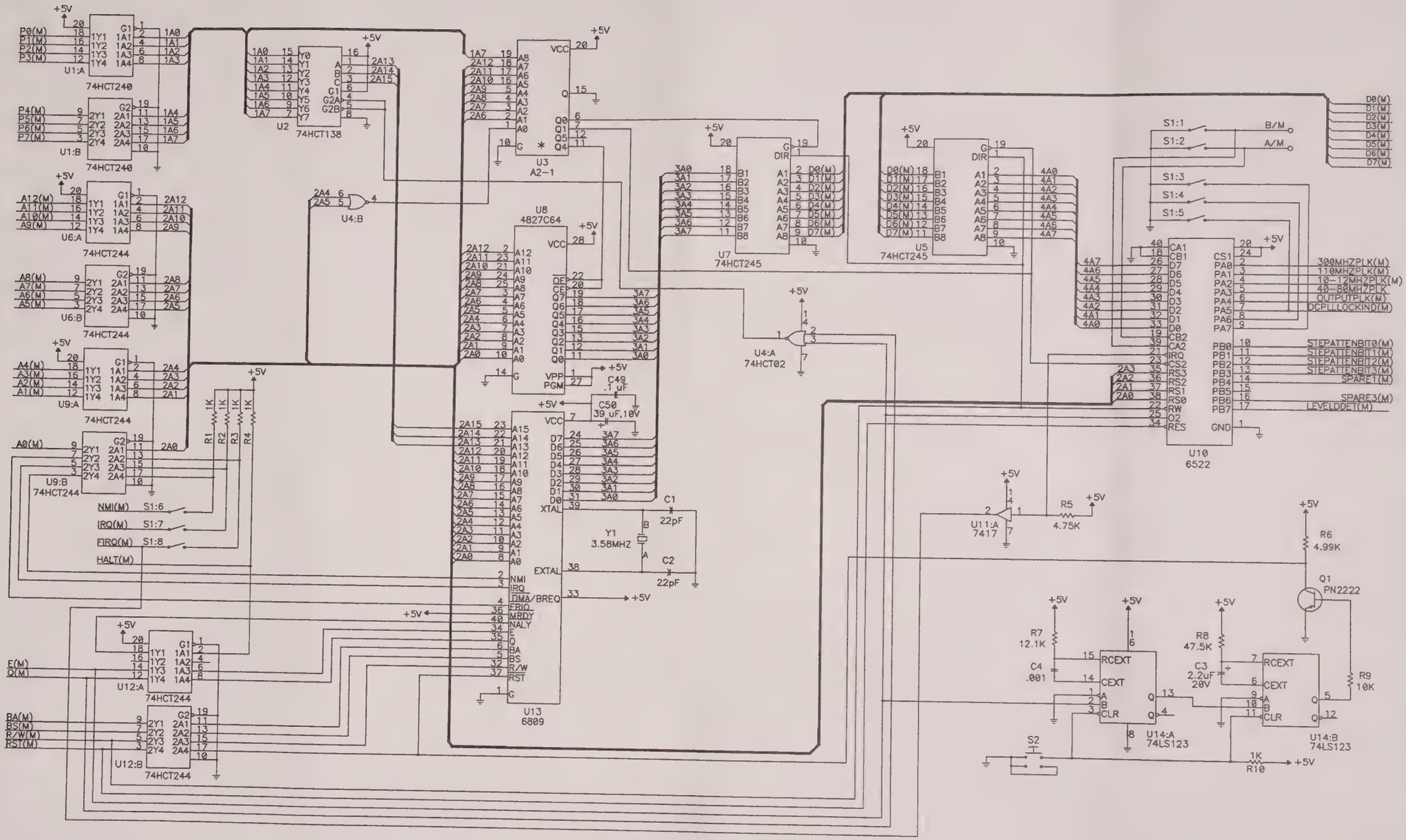
CPU -- PC ASSY A4

This board houses the two microprocessors. The master processor controls frequency synthesis, leveling, and modulation functions. The slave processor is used mainly to control radar simulation and measurement functions. The slave portion of the circuit (page 4) is a duplicate of the master portion of the circuit (page 3); the following description of the master side of the circuit also applies to the slave side, except that the component callouts have different numbers.

U13 is a 6809 microprocessor, which has a 16-bit address bus, and can address up to 64K of memory. It has an internal clock, regulated by crystal Y1 at 3.58 MHz (this frequency was chosen in order to avoid generating beat frequencies between its harmonics and the various reference signals produced within the instrument, most of which are exact multiples of 1 MHz). Multivibrator U14 furnishes a reset low-going pulse to the microprocessor upon power-up or whenever S2 is pressed.

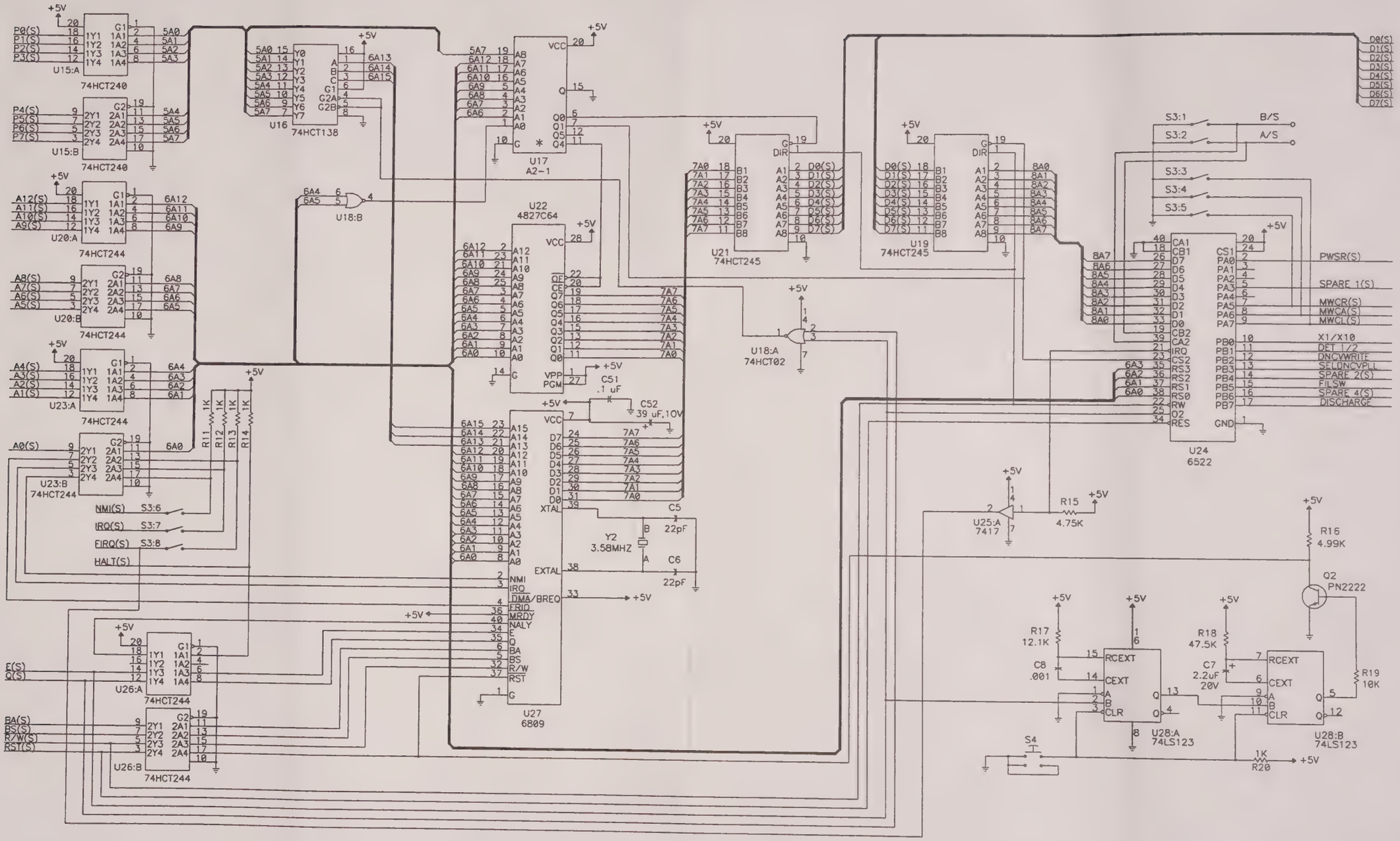
U8, a PROM having a capacity of 8K bytes, holds the instrument's initialization memory; it includes characterization data and other information unique to the individual instrument in which it is installed. Output buffers U1, U6, U9, and U12 connect the microprocessor's address bus and control lines with the computer bus. Address decoding is aided by the 3-to-8 line decoder, U2, which converts the three high-order address lines to eight page-lines. The computer uses these page-lines to select peripheral devices on other circuit boards. Within this circuit board, device address decoding is performed by U3, a high-speed bipolar PROM, whose decoded outputs drive the chip select lines and data direction select lines of the board's other ICs. The microprocessor's data bus is connected to the computer bus, and to input/output device U10, via bi-directional gates U7 and U5.

U10 is a programmable I/O device through which information is transmitted between the microprocessor data bus and other circuits. It is used for a number of instrument control and monitoring functions, such as programming the 10 dB step attenuator and polling the various PLL "lock" indicators.



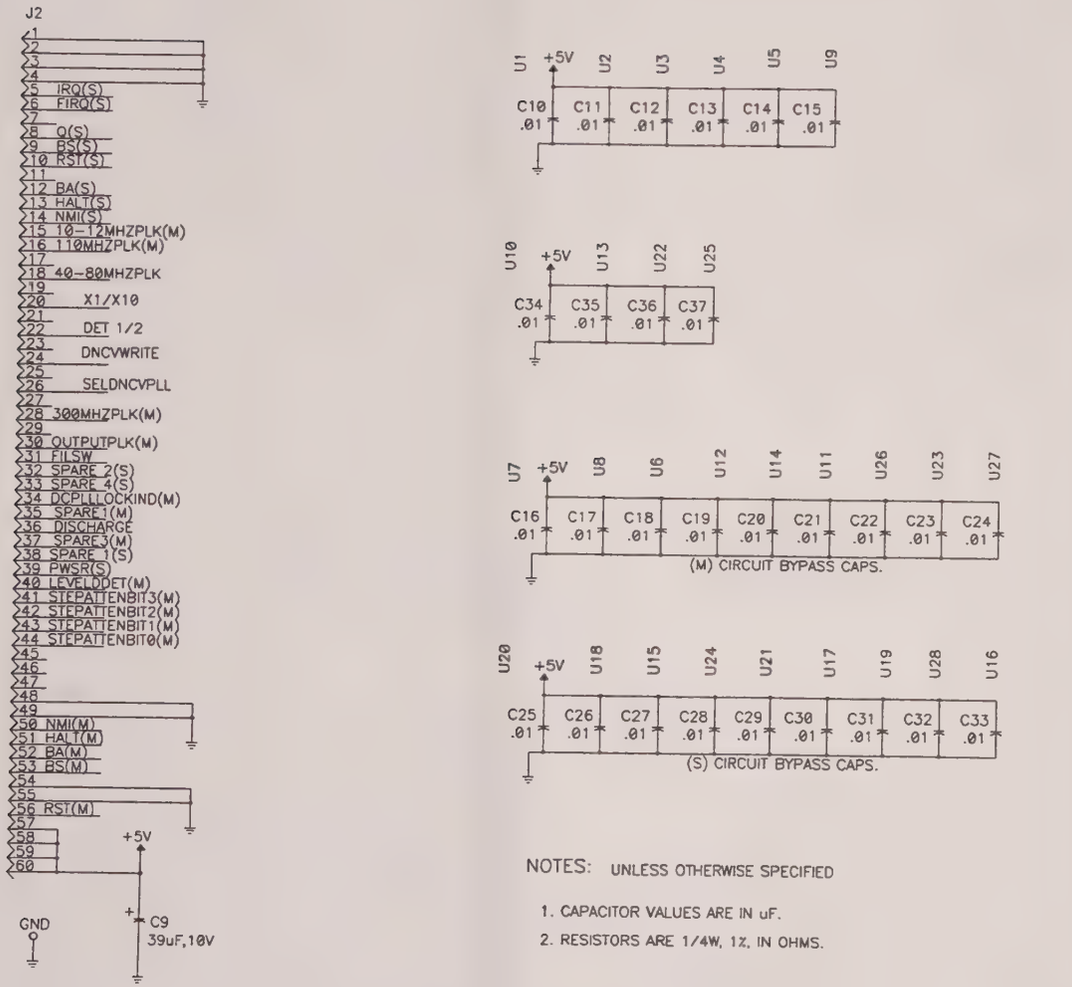
Dual Microprocessor CPU (A4)

DWG# 310BM15100 Rev B



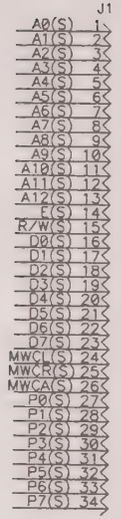
Dual Microprocessor CPU (A4)

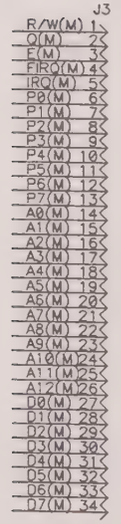
DWG# 310BM15100 Rev B



NOTES: UNLESS OTHERWISE SPECIFIED

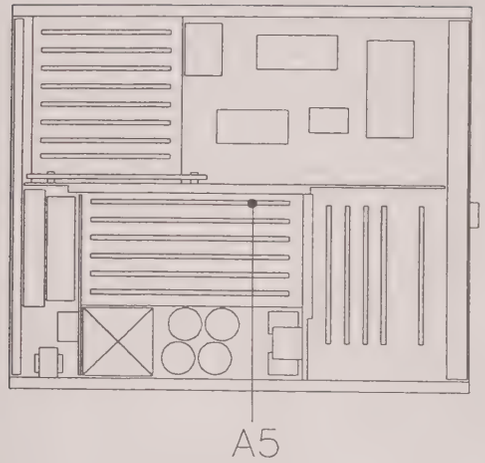
1. CAPACITOR VALUES ARE IN uF.
2. RESISTORS ARE 1/4W, 1%, IN OHMS.





Dual Microprocessor CPU (A4)

DWG# 310BM15100 Rev B

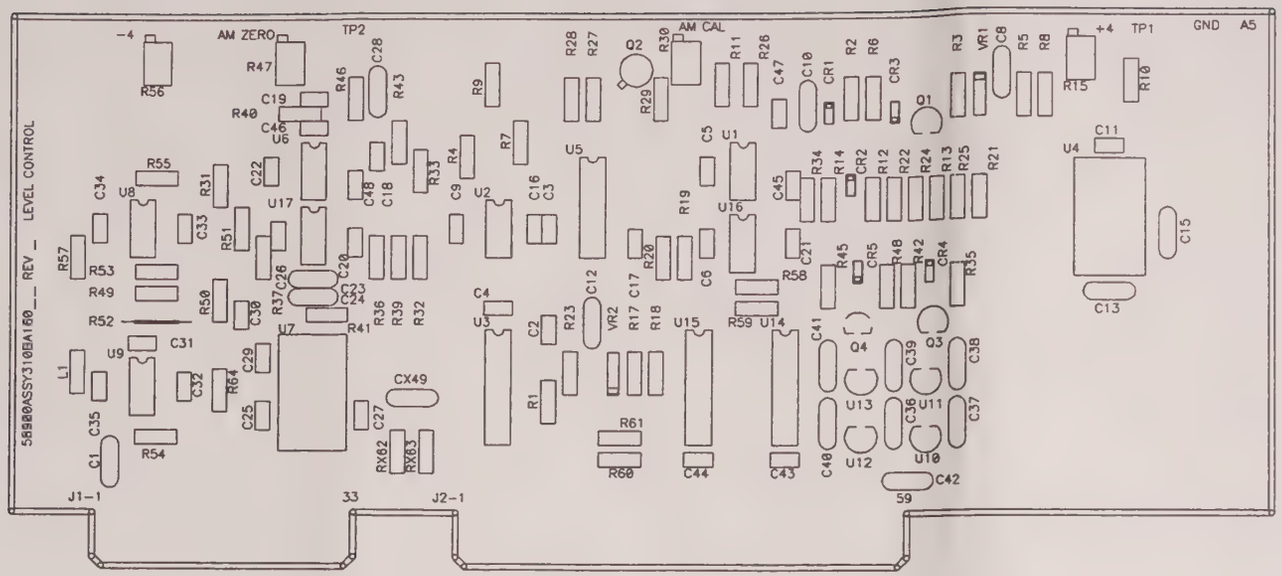


Level Control (A5)

DWG# 310BM16000 Rev A

Sheet 1 of 4

7-A5-1



LEVEL CONTROL -- PC ASSY A5

This circuit furnishes a control output to the leveling module which is derived from various control and correction inputs. In addition, this circuit drives the relays in the step attenuator.

The circuit shown on Sheet 3 runs the automatic level control (ALC) loop. U16B is the loop amplifier. All loop inputs are combined at the summing junction of U16-6. The amplifier output (U16-7) is boosted by the output stage (Q3, Q4, etc) to the levels required by the PIN diode leveler circuit. The LEVELING output typically has a range of roughly -1 to +15V; the output goes more positive to increase attenuation, more negative to reduce attenuation.

The input to the summing junction of U16-6 is a composite signal, of which the elements are: (1) a level reference set by the computer, (2) the amplitude modulation input, if any, and (3) feedback from the level detector in the RF output path. The loop amplifier output is driven so as to balance these inputs (that is, the attenuation of the leveler is adjusted so that the detector feedback signal equals the sum of the level reference and AM signals).

The computer specifies the level reference by programming U3, a multiplying DAC, with a multiplier. The DAC's output is proportional to the reference voltage at U3-15 (-6.2V) multiplied by the factor specified by the computer. The DAC output passes through the inverting amplifier U2. Using data in its level characterization table, the computer specifies a reference value which will yield the desired level. The level reference is supplied to the summing junction of U1-6.

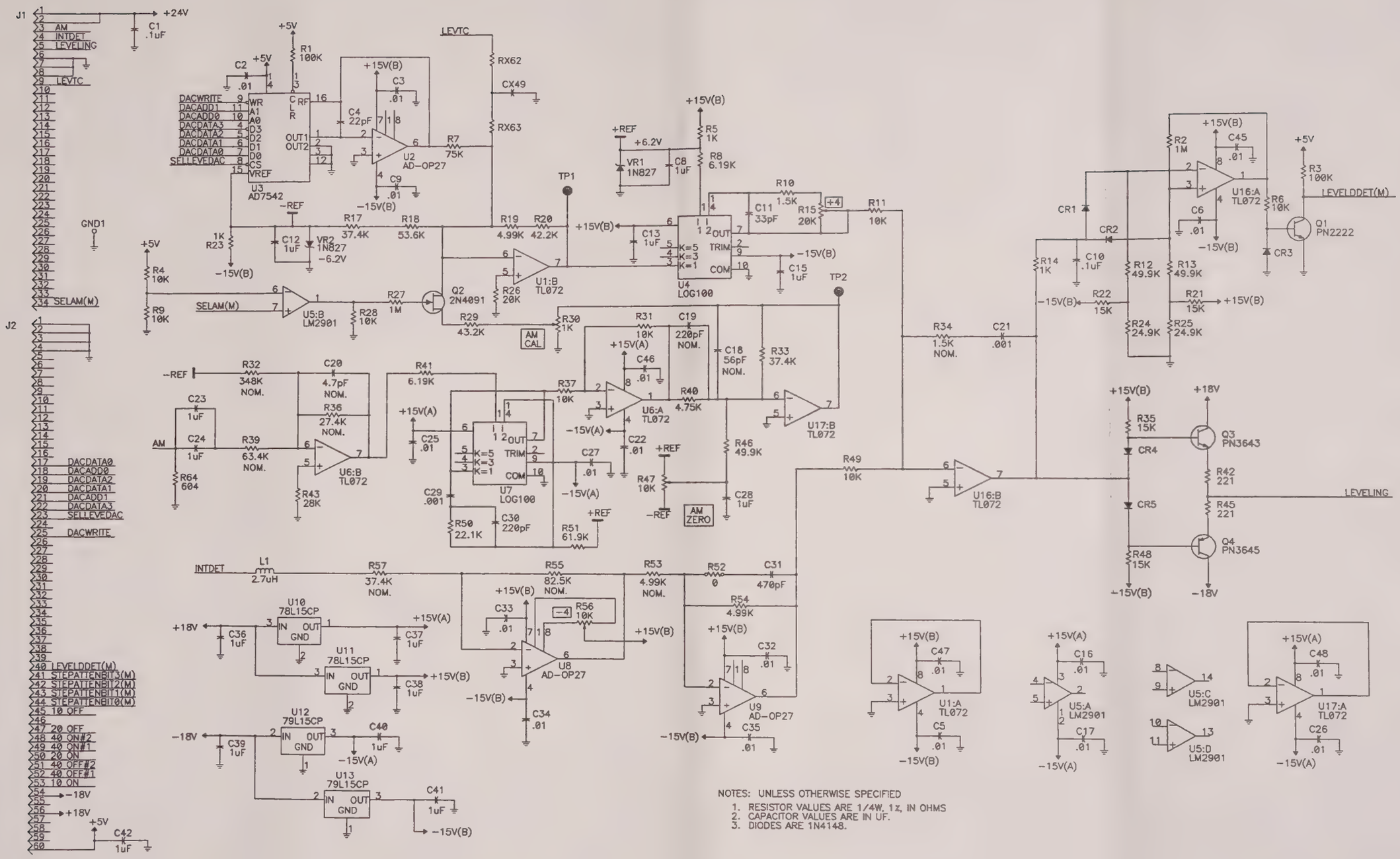
If the AM mode is selected, the computer uses the select line at U5-7 to turn Q2 on and so connect the AM branch to the summing junction of U1-6. The AM input from the front panel passes through four amplifiers (U6B, U7, U6A, and U17B) on the way to Q2. U7 is a logarithmic amplifier; it is needed because of the requirment for a logarithmic power characteristic in amplitude modulation.

The combined level reference and AM input pass through U1B to U4, an antilog amplifier. The purpose of U4 is to modify the linear charateristic of the DAC level reference so that it complements the log characteristic of the level detector. The AM input has already been given a log characteristic by U7, but that first stage only provided a logarithmic voltage curve; the logarithmic power curve required for amplitude modulation is provided by U4. The ouptut of U4 is supplied to the summing junction of the loop amplifier (U16-6).

Feedback received from the level detector (INT DET) is amplified by U8 and U9 and supplied to the summing junction of the loop amplifier (U16-6).

If the loop amplifier output at U16-7 is driven out of range, the circuit consisting of U16A and Q1 detects this "unleveled" condition and the LEVELDDET line goes low.

The circuit shown on Sheet 4 drives the relays in the 10 dB step attenuator; U14 and U15 convert the computer's attenuator setting control lines to the voltage levels required by these relays.



NOTES: UNLESS OTHERWISE SPECIFIED

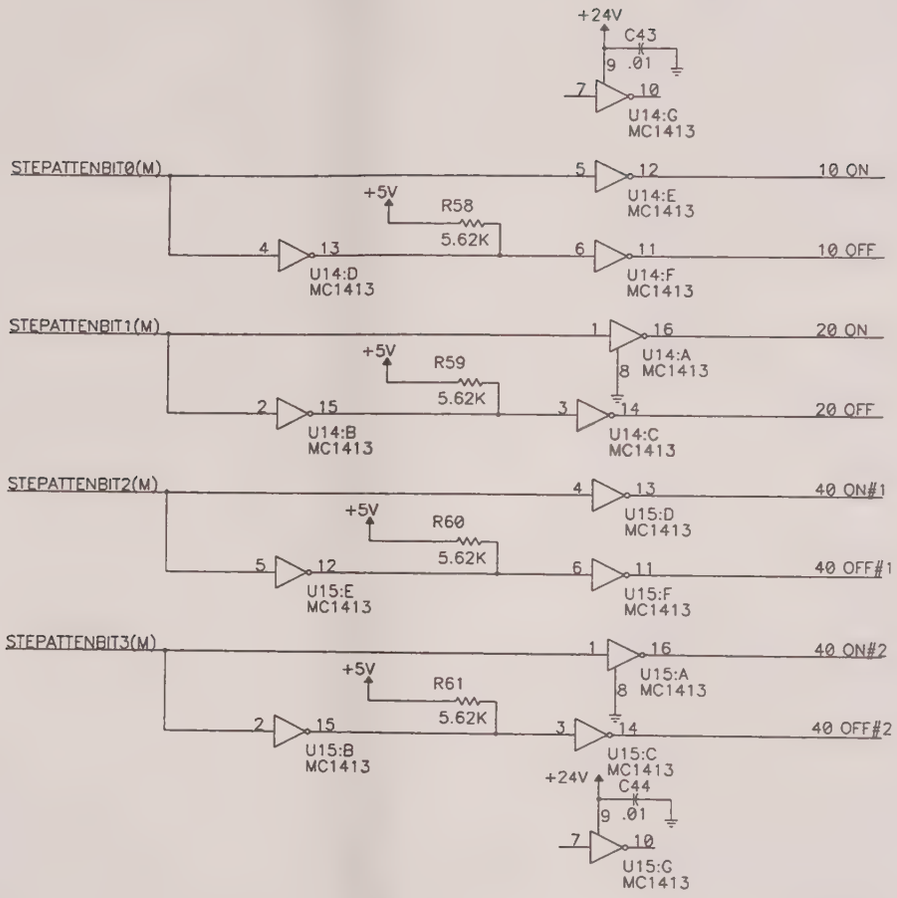
1. RESISTOR VALUES ARE 1/4W, 1%, IN OHMS
2. CAPACITOR VALUES ARE IN UF.
3. DIODES ARE 1N4148.

Level Control (A5)

DWG# 310BM16000 Rev A

Sheet 3 of 4

7-A5-3

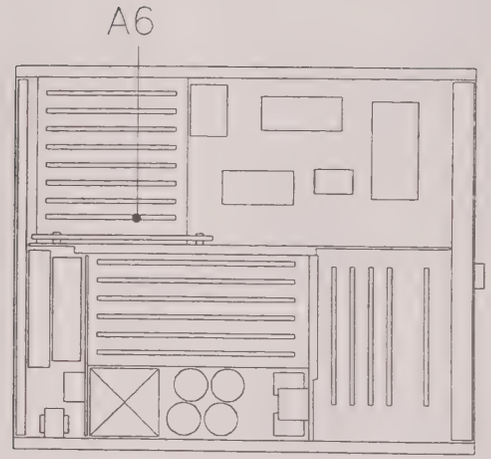


Level Control (A5)

DWG# 310BM16000 Rev A

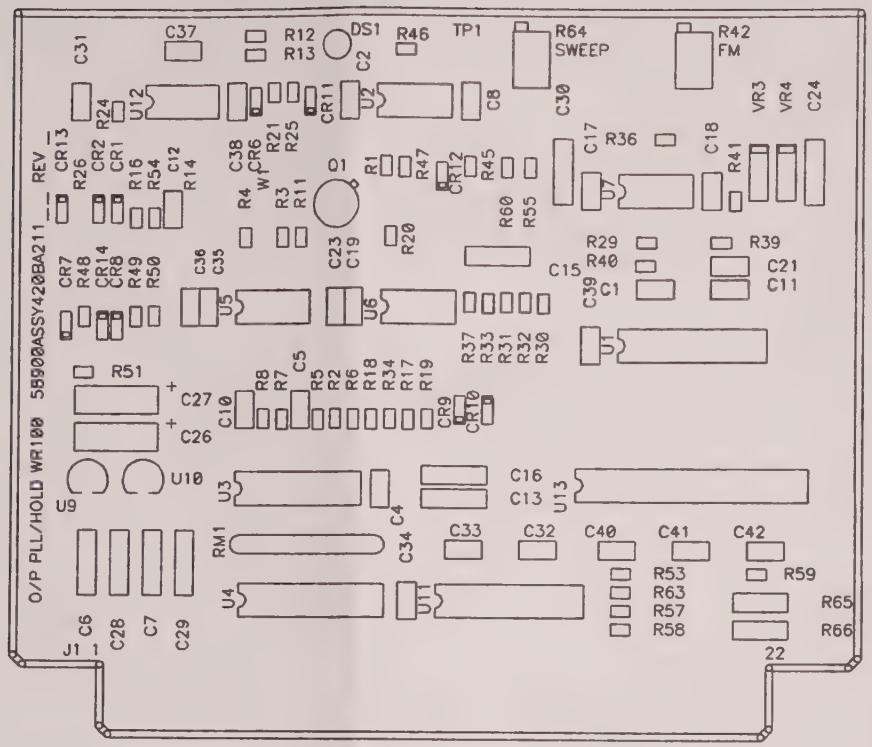
Sheet 4 of 4

7-A5-4



Output PLL (A6)

DWG# 420BM21101 Rev B



OUTPUT PLL -- PC ASSY A6

This circuit produces a control signal for use in fine-tuning the instrument's RF output VCO, in order to phase lock the VCO frequency to the master reference. During frequency modulation, the control signal is combined with an FM input.

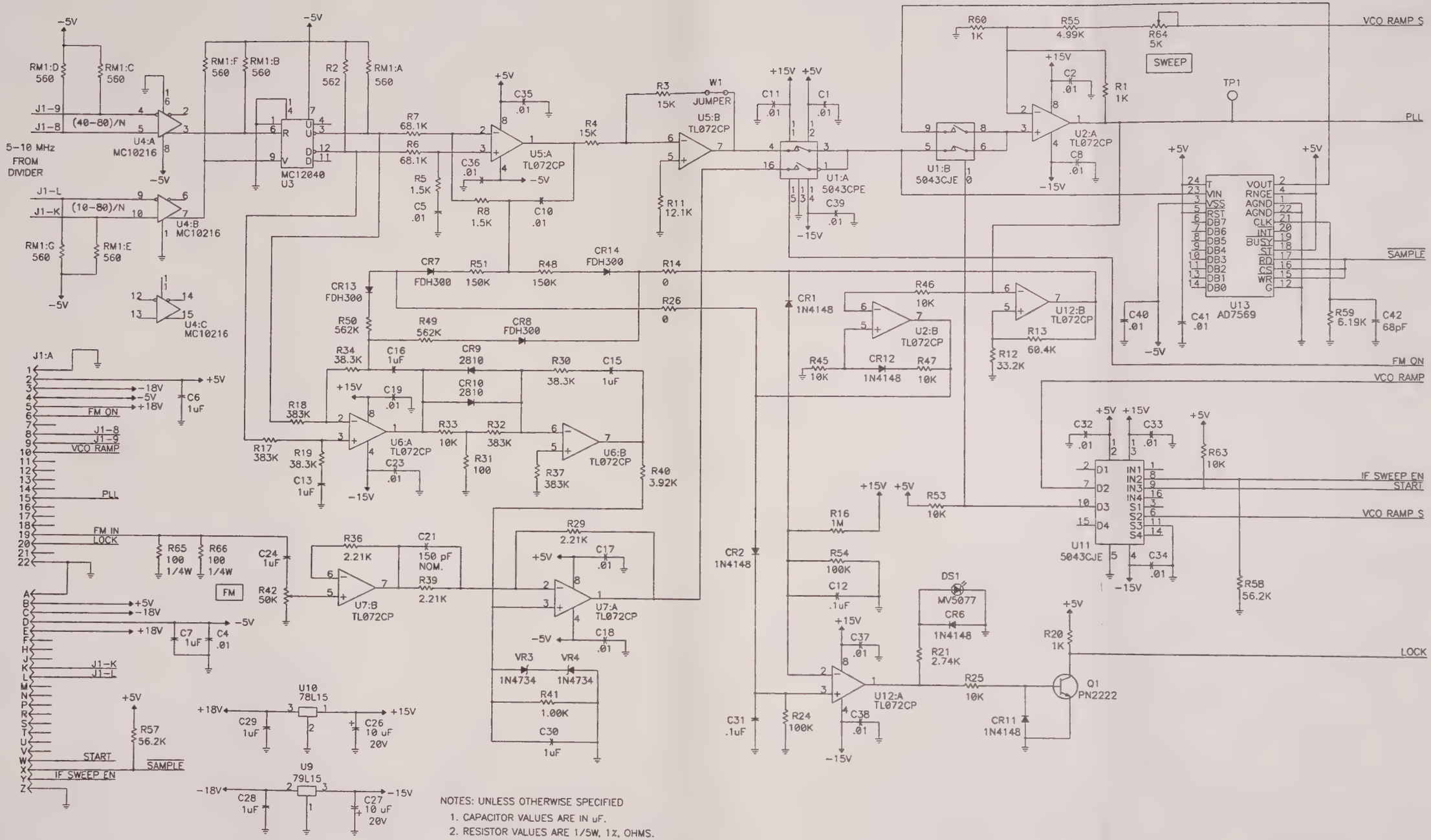
The phase detector (U3) receives two input frequencies, both of which are in the 5-10 MHz range; when the loop is locked these frequencies are equal. The reference frequency input (fR) comes from the divide-by-8 circuit on the divider board (A7), and the variable frequency input (fV) comes from the divide-by-N circuit on the same board. The phase detector produces outputs at pins 3 and 12 of U3; if the input frequencies are not in phase, wide pulses appear at one of these pins, depending on whether fV is leading or lagging. The outputs are used by the lock detector circuit (see U12:A, Q1) to determine whether the loop is locked. The outputs are used by the loop amplifier circuit to produce the loop's control output.

The phase detector outputs are amplified by U5-1 and U5-7; frequency compensation networks (R8/C10 and R5/C5) provide the rolloff needed to stabilize the loop. The output of U5-7 is applied (through the analog gate, U1) to the output amplifier, U2A. This output is used by the VCO driver board (A13) to tune the RF output VCO; it goes more negative to increase frequency, more positive to reduce frequency.

The second loop amplifier circuit, consisting of U6A & U6B, is used only during frequency modulation. The amplified phase detector output from U6-B is applied to amplifier U7A, where it is summed with the FM input signal, as amplfied by U7B. The output of U7A, which combines the modulation input with the phase detector output, is applied to switch U1A; during FM operation this combined signal is substituted for the phase-detector-only signal from U5B.

The variable frequency input to the phase detector is derived from the sampling mixer's IF, not directly from the VCO output. The mixer IF is the product of a harmonic multiplier, and may be derived from the wrong harmonic. In that case, the phase lock loop is misdirected, tuning the VCO in the wrong direction until it meets its positive or negative rail. To prevent the PLL from becoming stuck in this mode, a search circuit is added. This consists of amplifiers U2B and U12B, which monitor the circuit output and return control voltages to the loop amplifier circuits. When the output becomes too positive (minimum frequency), U12B swings to its negative rail, driving the output negative (maximum frequency). When the situation is reversed, U2B drives the output positive (minimum frequency).

During operation in the IF sweep mode, the phase detector is not used; a sample/hold circuit (seeU13) provides a fixed level equal to the previous loop output to swtich U1B. The sample/hold output is summed with a sweep ramp input, with the result that the output of U2A ramps upward from the "hold" level.



NOTES: UNLESS OTHERWISE SPECIFIED

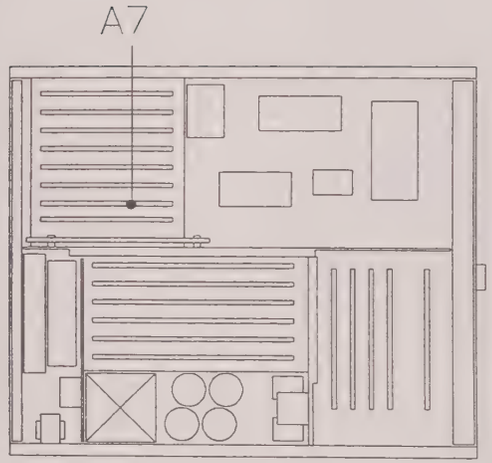
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE 1/5W, 1%, OHMS.

Output PLL (A6)

DWG# 420BM21101 Rev B

Sheet 3 of 3

7-A6-3

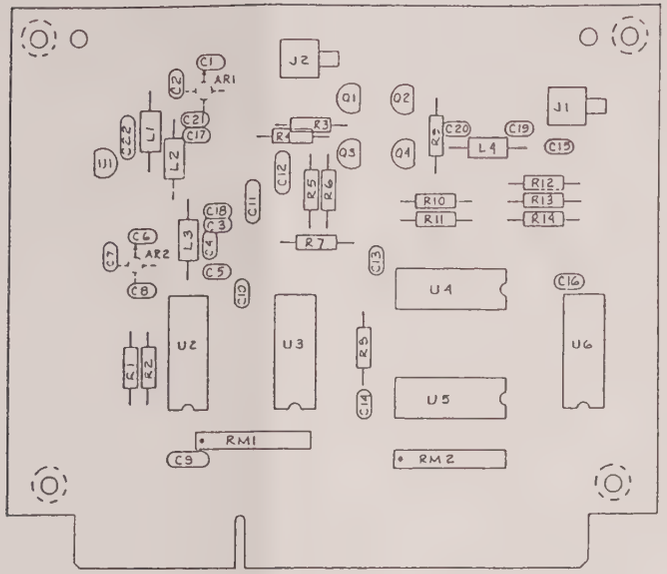


Divider (A7)

DWG# 304BM03110 Rev A

Sheet 1 of 3

7-A7-1



Divider (A7)

DWG# 304BM03110 Rev A

Sheet 2 of 3

7-A7-2

DIVIDER -- PC ASSY A7

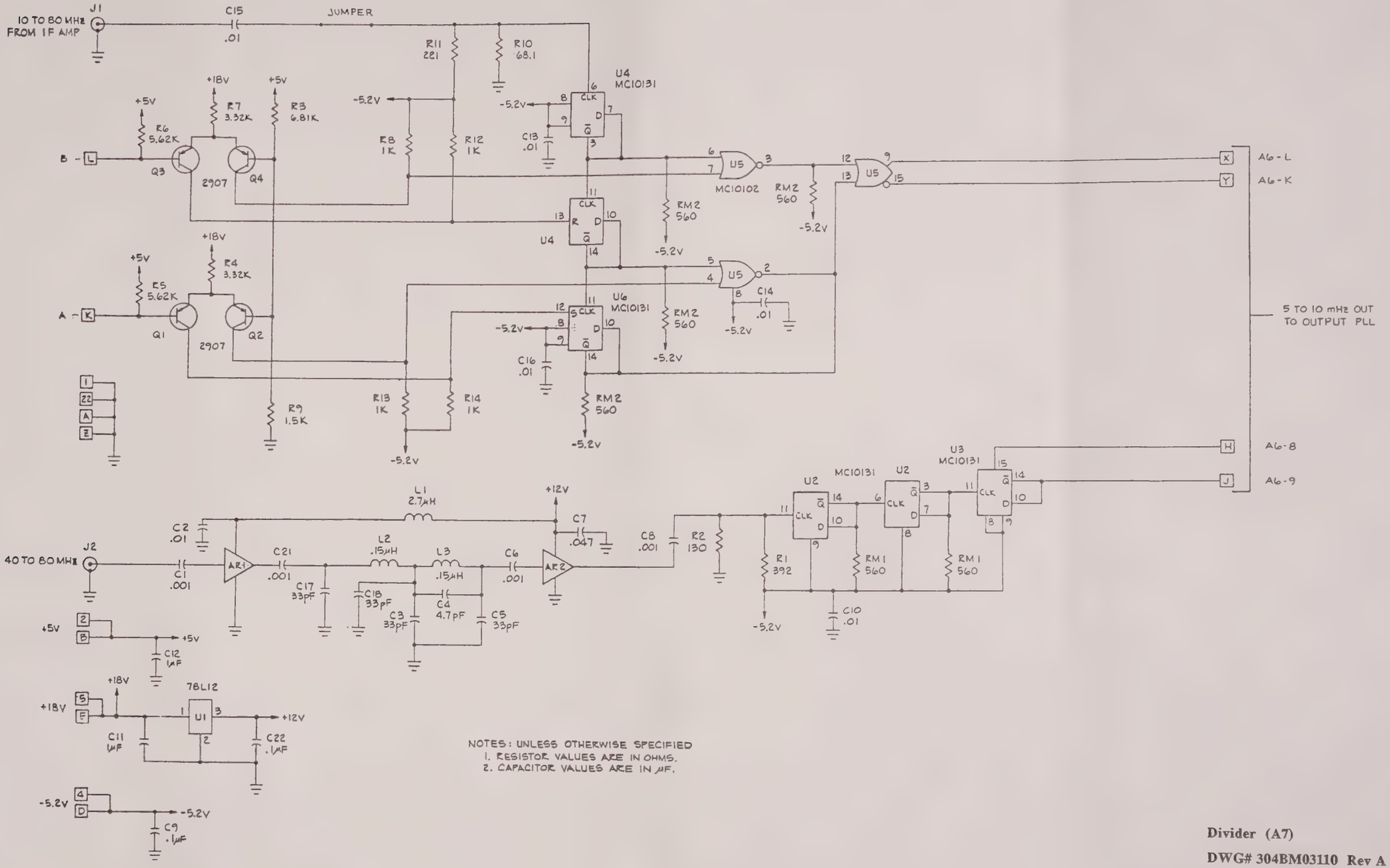
This circuit includes two frequency dividers, one fixed and one programmable, which supply paired 5-10 MHz signals to the output PLL circuit (A6).

The fixed frequency divider has a divisor of 8. It accepts an input frequency from the 40-80 MHz PLL circuit (A8). The input frequency is applied to a low-pass filter (L2/L3, etc.), and to amplifiers AR1 and AR2. The amplified 40-80 MHz signal is used to clock a series of three flip flops (U2, U3). The output of the third flip flop is the input frequency divided by 8 (in other words, it has a range of 5-10 MHz).

The programmable divider circuit can be set to divide by 2, 4, or 8. It accepts a 10-80 MHz sampler IF from the 300 MHz Oscillator board (A202). A low pass filter (L4, etc.) removes spurious high frequencies from the signal. A series of three flip flops (U4, U6) is used to provide three outputs equal to the input frequency divided by 2 (at U4-3), by 4 (at U4-14), and by 8 (at U6-14). The computer selects the appropriate divisor by means of the 'A' and 'B' control inputs. Because these inputs are at TTL logic levels, two differential amplifiers (Q1/Q2, and Q3/Q4) are used to convert them to ECL voltages. The differential outputs drive the SET and RESET inputs at U4-13 and U6-12, and also to drive the steering gates at U5-7 and U5-4. Only one of the three flip flops is allowed to contribute its output to the final buffer, U5-9.

The computer selects a divisor which will reduce the 10-80 MHz IF input to a 5-10 MHz output. The 'A' and 'B' control bits (see Q1 and Q3) are interpreted as follows:

'A'	'B'	DIVISOR
0	0	2
0	1	4
1	1	8



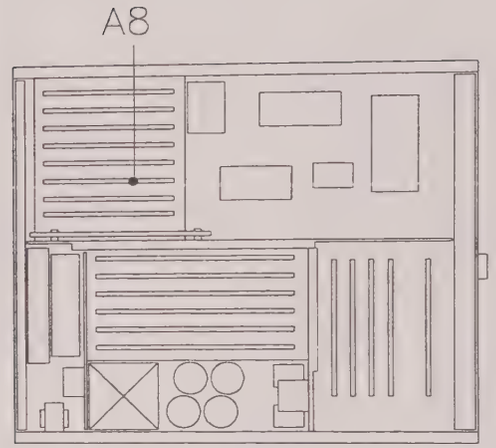
NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS.
2. CAPACITOR VALUES ARE IN μF.

Divider (A7)

DWG# 304BM03110 Rev A

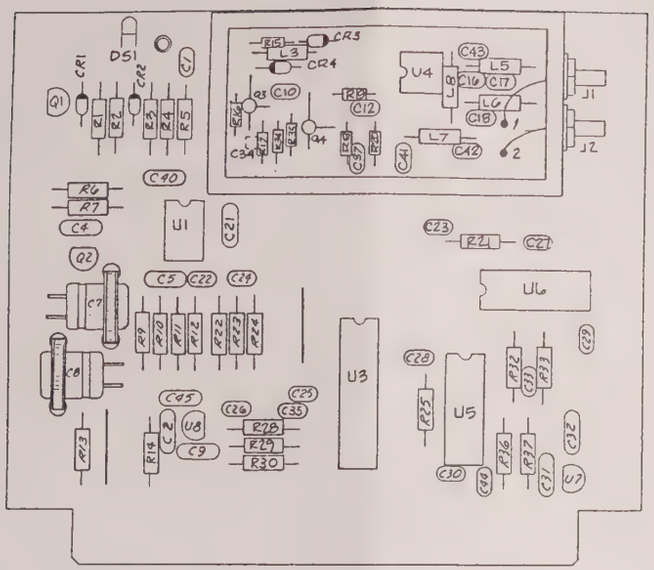
Sheet 3 of 3

7-A7-3



40-80 MHz Phase Lock Loop (A8)

DWG# 304BM03000 Rev K



40-80 MHz Phase Lock Loop (A8)

DWG# 304BM03000 Rev K

Sheet 2 of 3

7-A8-2

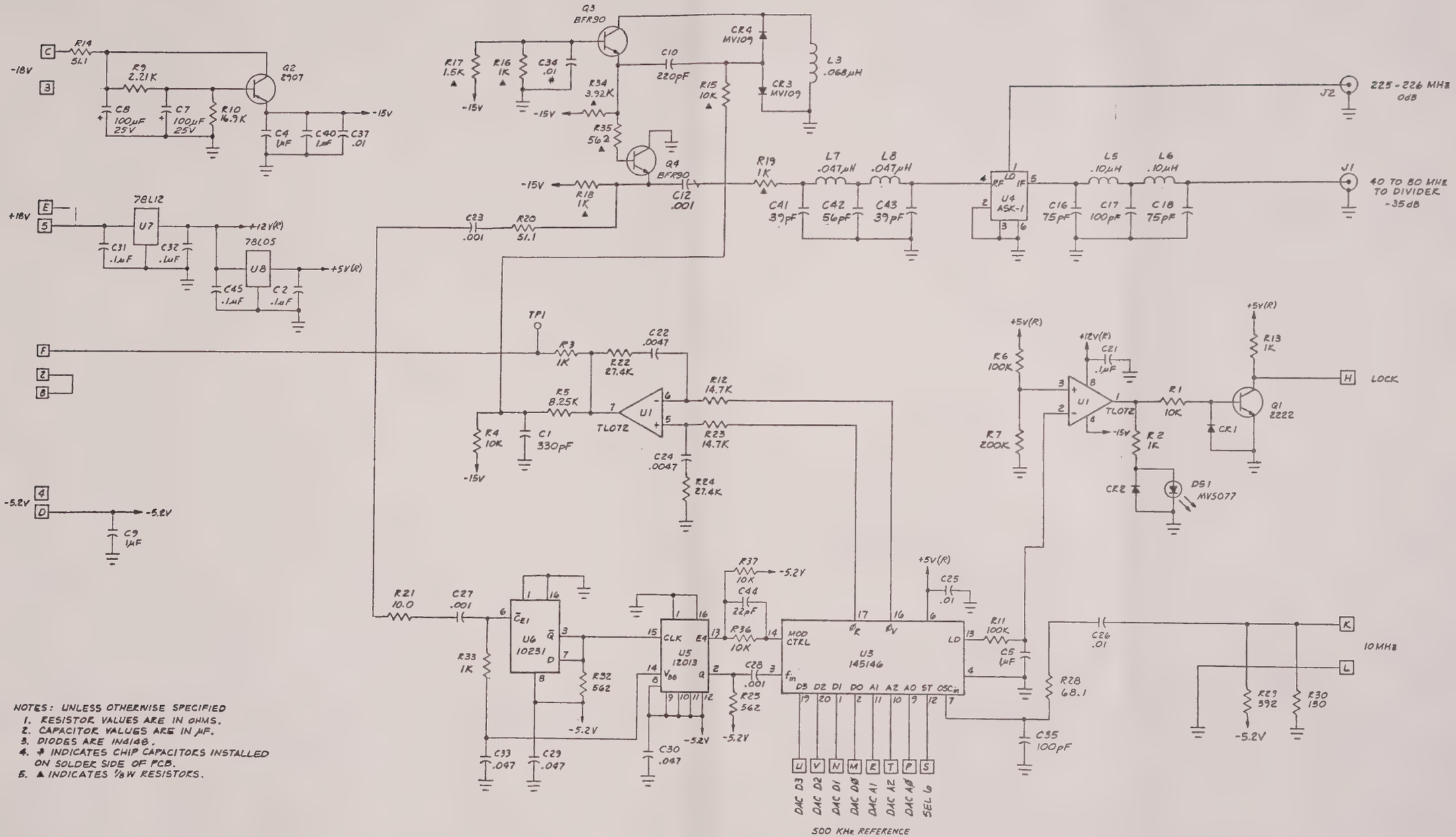
40-80 MHz PLL -- PC ASSY A8

This circuit provides a programmable reference frequency to the instrument's output phase lock loop. The 40-80 MHz circuit output at J1 is an intermediate frequency produced by mixer U4; it is equal to the difference between the 220 MHz input (J2) and the frequency produced by the VCO (Q3). A low pass filter (L5, etc.) removes spurious high frequencies from the IF output. The VCO has a range of 145-185 MHz, and is tuned by a phase lock loop circuit.

The PLL circuit is programmed by means of the MC145146 PLL chip, U3. This IC includes three programmable frequency counters: one for dividing the 10 MHz reference input, one for dividing the variable input (feedback from the VCO), and one for controlling an external prescaler (U6/U5) on the variable input. The IC's reference input (U3-7) is taken from the 10 MHz master reference input. The reference counter is programmed to divide the 10 MHz input by 40, for a 250 kHz input to the internal phase detector. The variable counter and the external prescaler counter (U6/U5) are used in combination to divide the VCO frequency, for a 250 kHz input to the internal phase detector when the loop is locked.

The phase detector outputs at U3-17 and U3-16 provide output pulses to indicate whether the variable frequency (derived from the VCO output) is leading or lagging the reference. These pulses are converted by loop amplifier U1-7 into a tuning voltage for the VCO. By programming U3's internal counters, the computer can select a VCO frequency in 1 MHz steps between 145 and 185 MHz.

U3's internal lock detector (pin 13) drives U1-1 and Q1 so that the DS1 is illuminated and the 'lock' output at pin H is low for the unlocked condition. In the locked condition, DS1 is dark and pin H is high.

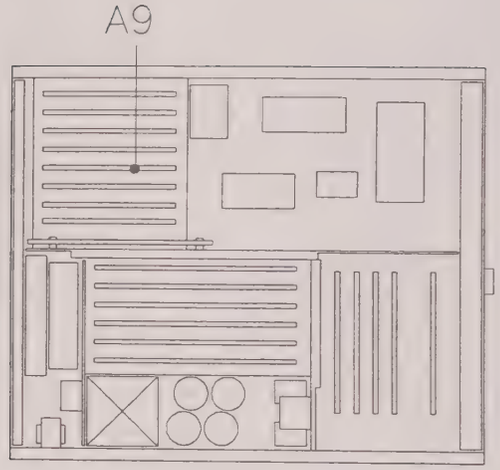


40-80 MHz Phase Lock Loop (A8)

DWG# 304BM03000 Rev K

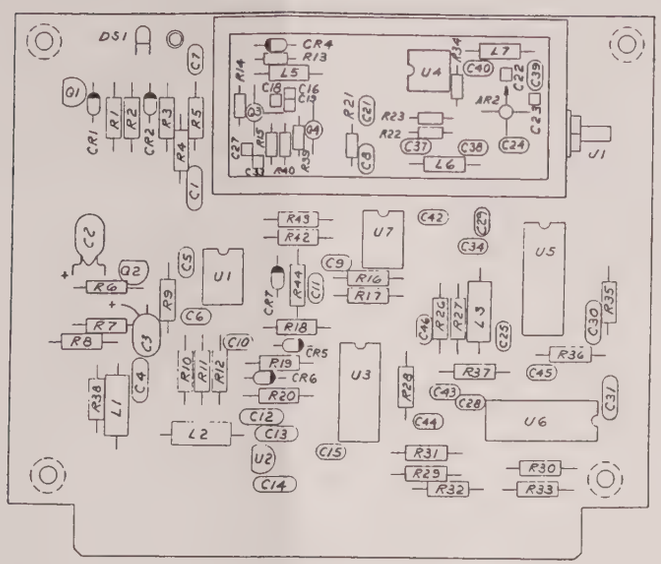
Sheet 3 of 3

7-A8-3



Intermediate Phase Lock Loop (A9)

DWG# 304BM02700 Rev H



Intermediate Phase Lock Loop (A9)

DWG# 304BM02700 Rev H

Sheet 2 of 3

7-A9-2

INTERMEDIATE PHASE LOCK LOOP -- PC ASSY A9

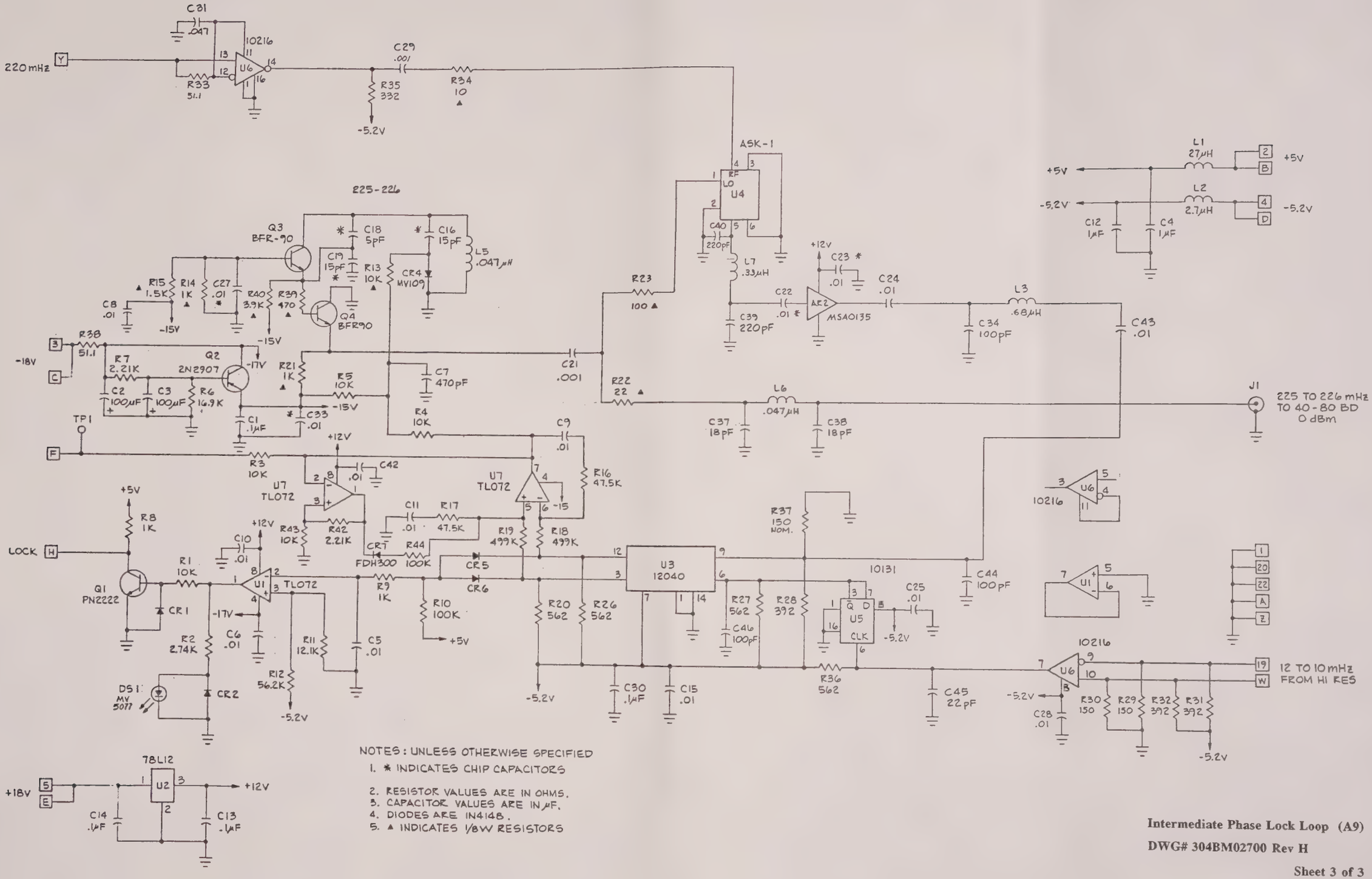
The function of this circuit is to synthesize frequencies between 225 and 226 (for use by the 40-80 MHz PLL), derived from reference inputs at 220 MHz and 10-12 MHz. The main elements of the circuit are the voltage controlled oscillator (VCO), the mixer, the phase comparator, and the lock detector.

The VCO (see Q3, etc.) is designed to oscillate at 225 to 226 MHz; its output frequency is determined by the tuning voltage received from U7-7 (the tuning voltage is measurable at TP1). The VCO output is furnished (through a low pass filter which eliminates harmonics) to connector J1. The VCO is also applied to the RF mixer (see U4).

The RF mixer combines the VCO frequency with the 220 MHz reference input frequency (buffered by U6-14), producing at U4-5 an intermediate frequency (IF) output equal to the difference between them, or 5 to 6 MHz. Since the 220 MHz input is fixed, the IF is determined entirely by the VCO output. The IF output is amplified (AR2), filtered (see L3, etc.), and applied to the variable input of the phase comparator (U3-9).

The phase comparator produces pulses at one of its outputs pins (U3-3 or U3-12) depending on whether its variable input (pin 9) is leading or lagging the reference input (pin 6). The reference input is at 5-6 MHz and is derived from the 10-12 MHz input from the high resolution PLL board (pins W and 19, buffered by U6-7 and divided in half by flip flop U5). The loop amplifier (U7-7) converts U3's output pulses into a DC control voltage for the VCO. The phase comparator tunes the VCO upward or downward in order to equalize its two input frequencies; when these two frequencies are equal, the loop is "locked". The output frequency of the circuit as a whole (J1) is therefore determined by the frequency of the 10-12 MHz input.

The phase comparator's output pulses are furnished (via CR5, CR6) to the lock detector circuit (see U1-2). When the loop is unlocked (i.e., when there is a large difference between the phase comparator's inputs) the output pulses become very wide, U1-1 goes high, turns on Q1 and fault indicator DS1, and pulls the 'LOCK' output (pin H) low.

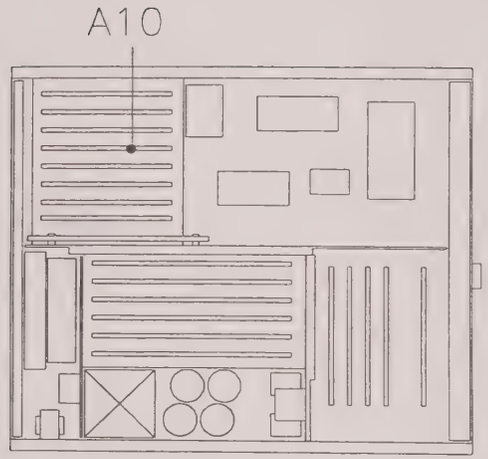


NOTES: UNLESS OTHERWISE SPECIFIED

1. * INDICATES CHIP CAPACITORS
2. RESISTOR VALUES ARE IN OHMS.
3. CAPACITOR VALUES ARE IN μF.
4. DIODES ARE IN4148.
5. ▲ INDICATES 1/8W RESISTORS

Intermediate Phase Lock Loop (A9)

DWG# 304BM02700 Rev H

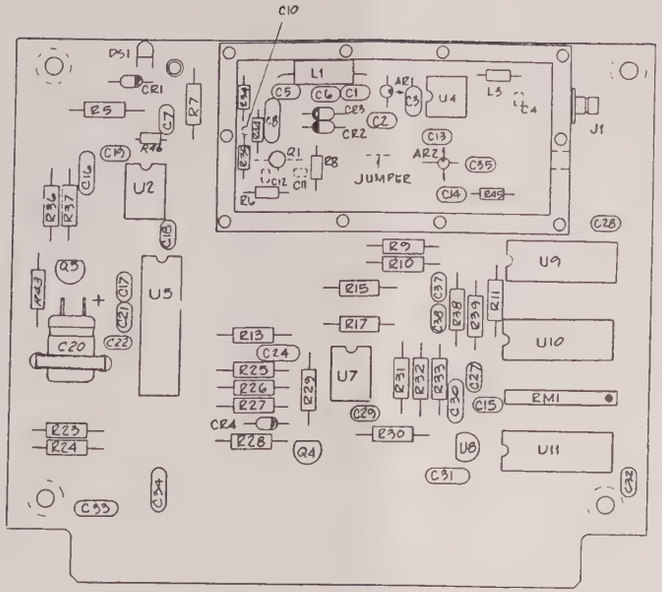


High Resolution (A10)

DWG# 304BM03410 Rev D

Sheet 1 of 3

7-A10-1



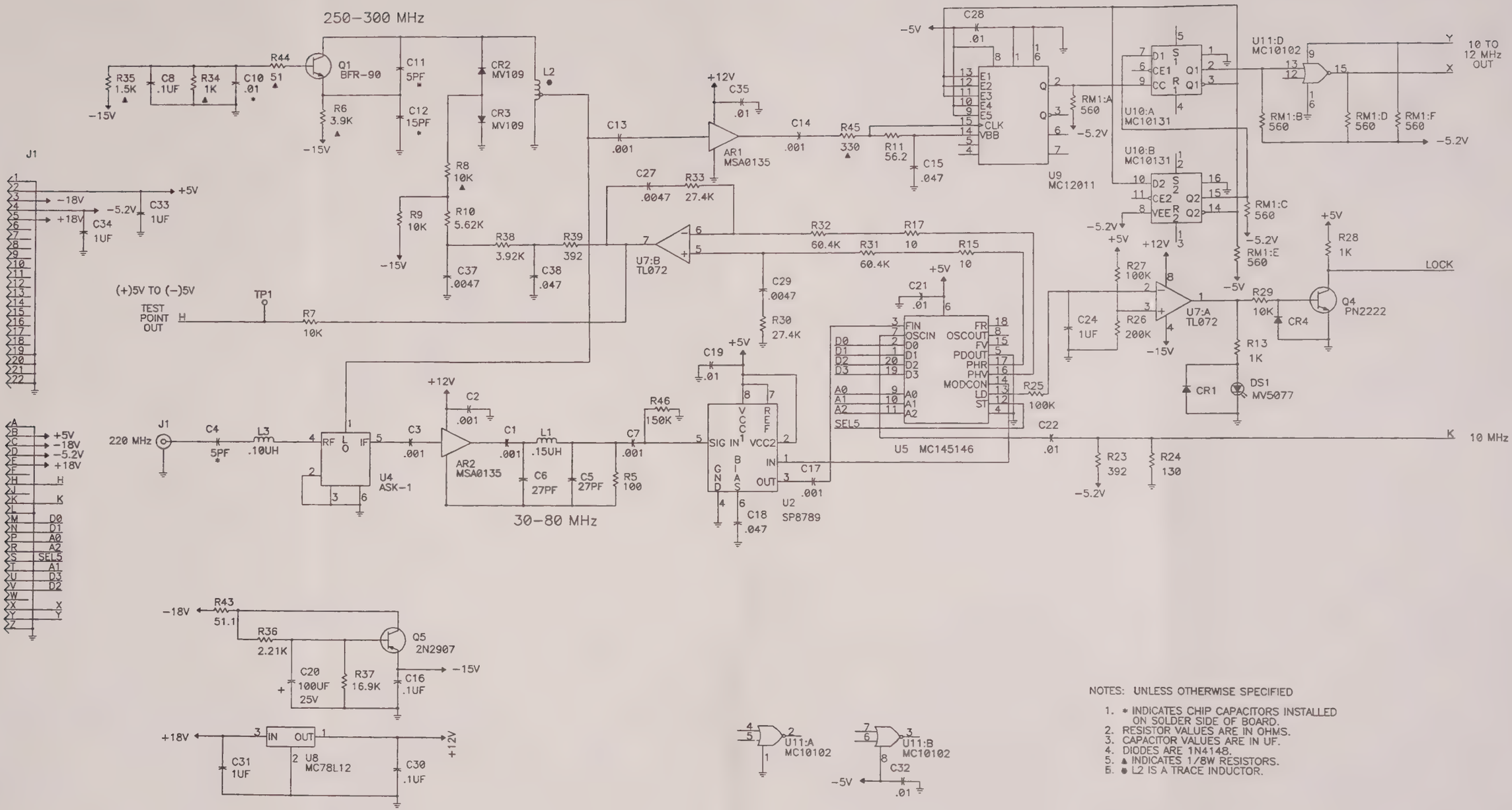
HIGH RESOLUTION -- PC ASSY A10

This circuit generates a reference frequency in the range of 10-12 MHz, programmable in steps of 2 kHz. A voltage controlled oscillator (Q1, etc.) produces a 250-300 MHz signal which, divided by 25 (U9, U10) yields the circuit's output frequency. A programmable synthesizer circuit tunes the VCO in order to generate a range of frequencies which are phase locked to the 10 MHz master reference. Because the VCO frequency is much higher than the master reference, it is mixed (U4) with the 220 MHz reference input to create a 30-80 MHz IF which is within the frequency range of the PLL circuit.

Synthesizer chip U5 contains three programmable counters and a phase detector. One internal counter divides the 10 MHz master reference by 200, yielding a 50 kHz reference for the phase detector. The remaining internal dividers are used in conjunction with the external prescaler divider (U2, which divides by either 20 or 21) in order to reduce the 30-80 MHz mixer IF to 50 kHz. One of its phase detector outputs (pins 16 or 17) will produce wide pulses to indicate that the divided IF from the mixer is leading or lagging the divided master reference. The loop amplifier (U7-7) turns the phase detector output pulses into a control voltage by which the VCO is tuned. The amplifier drives the oscillator in whichever direction will reduce the phase difference between the two phase detector inputs, until the VCO is phase locked to the master reference. U5's lock detector output (pin 13) is applied to the detector circuit (U7-1, Q4 etc.); the light emitting diode (DS1) is illuminated for the unlocked condition.

A sample of the VCO frequency is mixed (by U4) with the 220 MHz reference input; the resulting 30-80 MHz IF is amplified (AR1), filtered (L1 etc.) and applied to prescaler U2.

The output frequency of the VCO is tapped at L2, which is implemented as a printed trace on the circuit board. AR2 amplifies the VCO signal. The circuit consisting of U9 and U10 is a fixed frequency divider with a divisor of 25. U9 divides by either 8 or 9 (its divisor is programmed by the logic level fed back from U10-3). The two flip flops of U10 are used as a divide-by-3; U10-3 is low during one cycle out of three, programming U9 to divide by 9 for that period and by 8 the rest of the time, for a total division of the VCO frequency by 25. The 10-12 MHz quotient is buffered and complemented by U11.



NOTES: UNLESS OTHERWISE SPECIFIED

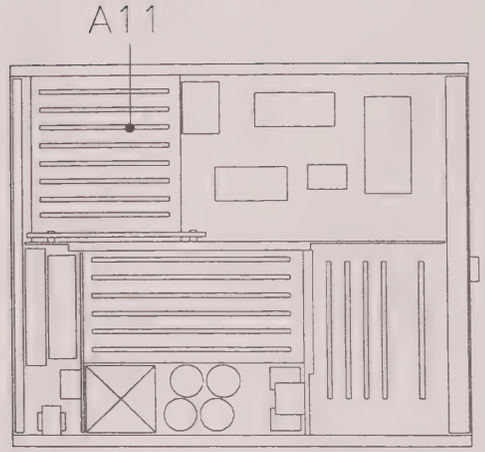
1. * INDICATES CHIP CAPACITORS INSTALLED ON SOLDER SIDE OF BOARD.
2. RESISTOR VALUES ARE IN OHMS.
3. CAPACITOR VALUES ARE IN UF.
4. DIODES ARE 1N4148.
5. ▲ INDICATES 1/8W RESISTORS.
6. ● L2 IS A TRACE INDUCTOR.

High Resolution (A10)

DWG# 304BM03410 Rev D

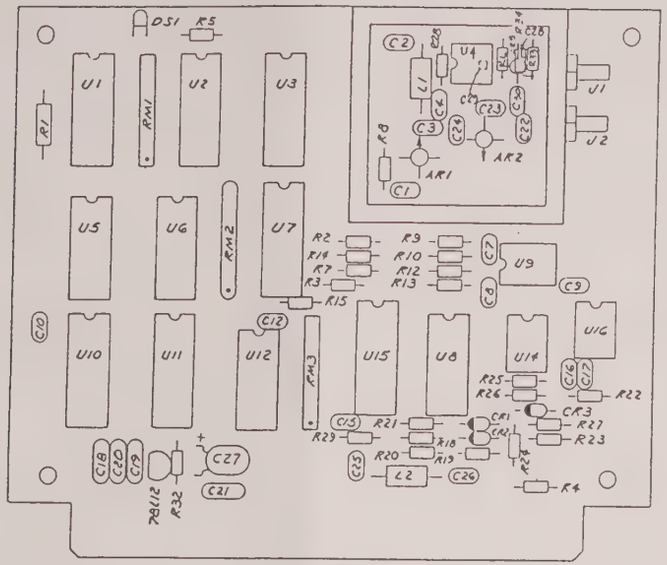
Sheet 3 of 3

7-A10-3



300 MHz Phase Lock Loop (A11)

DWG# 304BM02200 Rev K



300 MHz Phase Lock Loop (A11)

DWG# 304BM02200 Rev K

Sheet 2 of 4

7-A11-2

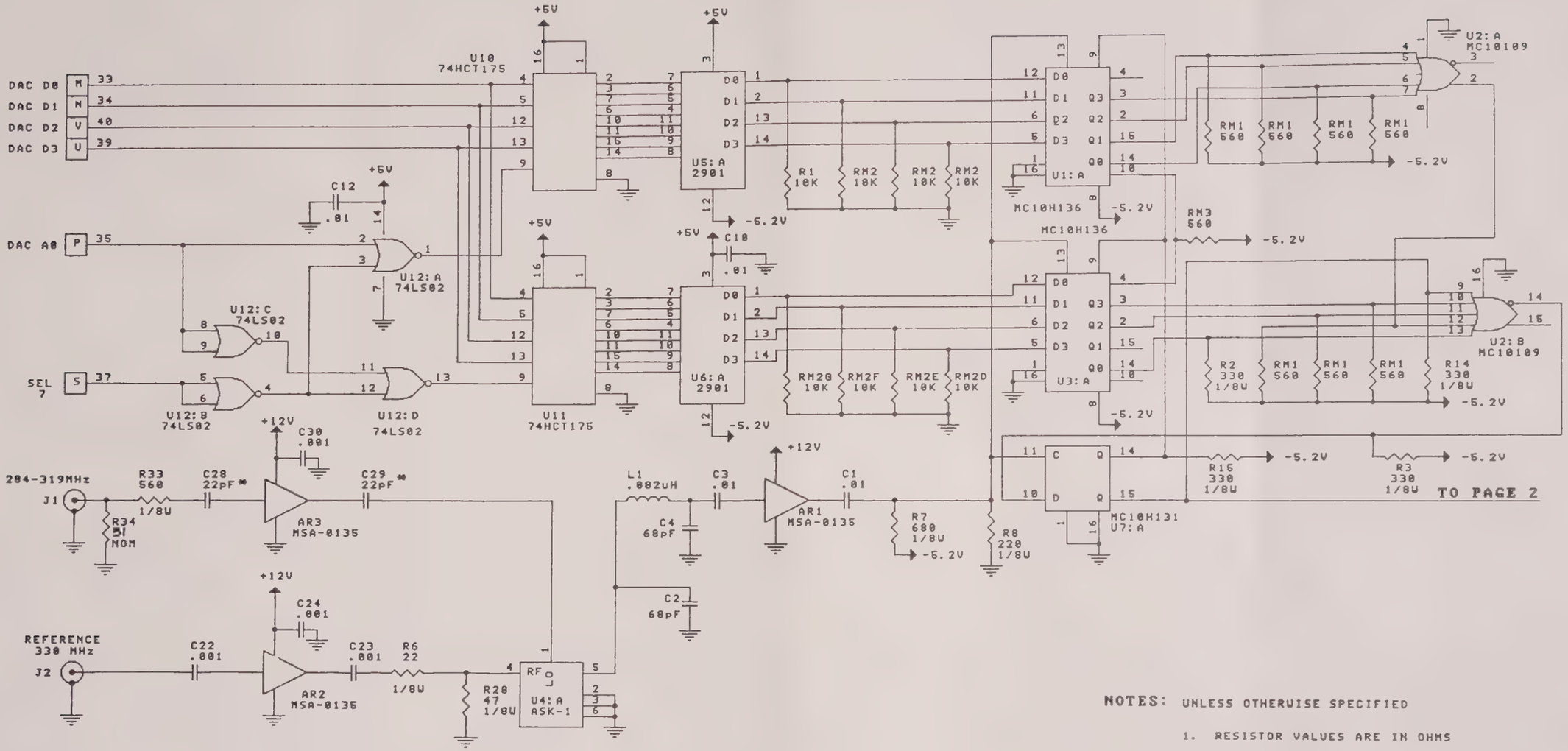
300 MHz PHASE LOCK LOOP -- PC ASSY A11

This circuit tunes the 300 MHz voltage controlled oscillator (PC board A202). The VCO can be programmed over a range of 284 to 319 MHz; the PLL circuit enables the computer to select the desired VCO frequency and phase lock the VCO to the instrument's 10 MHz timebase. The input at J1 is feedback from the VCO. Because the 284-319 MHz input frequency is too high to be counted by the digital circuits used here, the input signal is mixed (see U4) with the 330 MHz reference input (received at J2 and amplified by AR2) yielding an intermediate frequency in the range of 11-46 MHz. A low pass filter (L1 etc.) removes the mixer input frequencies. The IF is then amplified (AR1) and applied to the programmable divider.

The purpose of the programmable divider is to divide the 11-46 MHz IF down to 1 MHz. The first stage of the divider consists of latches U10 and U11; the computer selects the divisor (in the range of 11-46) by loading it as two successive four-bit words into these latches (U12 drives the chip select lines of the latches). The complementary outputs of the latches are applied to the comparators of U5 and U6; the comparator outputs translate the eight-bit divisor into ECL levels for use by the high speed ECL down-counters, U1 and U3. The counters are clocked by the amplified IF, and count down from the numbers programmed into them. U3 represents the four least significant bits, U1 the four most significant bits. Flip flop U7, also clocked by the IF, receives a high at its 'D' input (U7-10) at the end of the count and sends a high output pulse (from U7-15) to the phase comparator. The counters are reset by U7-14 and the count repeats.

The phase comparator chip, U8, requires reference and variable frequency inputs. The reference input is derived from the instrument's 10 MHz timebase. The 10 MHz input is received at pins K and L, filtered (L2 etc.) and divided by ten at U15. The 1 MHz quotient is applied to the comparator at U8-6. The variable input, received from the programmable divider circuit (see U7-15), is applied to the comparator at U8-9. The phase comparator produces wide pulses at one of its outputs (pin 3 or 12) depending on whether the variable input is leading or lagging the reference. The loop amplifier circuit (U16 etc.) converts these pulses into a DC voltage output (pins W, X) with which to tune the VCO. The polarity of tuning is: more positive to increase frequency, more negative to decrease frequency. The PLL circuit tunes the VCO in whatever direction will reduce the phase difference between the reference and variable inputs to the comparator. Filter components in the loop amplifier circuit (C16, C17, etc.) remove the phase comparator's output pulses from the tuning signal.

When there is a large phase difference between the reference and variable inputs to the comparator (i.e., when the loop is "unlocked"), wide low-going pulses appear at one of U8's outputs. These pulses are detected by the circuit consisting of U9 etc., and cause the 'LOCK' output at pin Y to go low and the LED (DS1) to be lit. When the loop is locked, U8's output pulses become extremely narrow and shallow, the 'LOCK' output is high, and the LED is extinguished.



NOTES: UNLESS OTHERWISE SPECIFIED

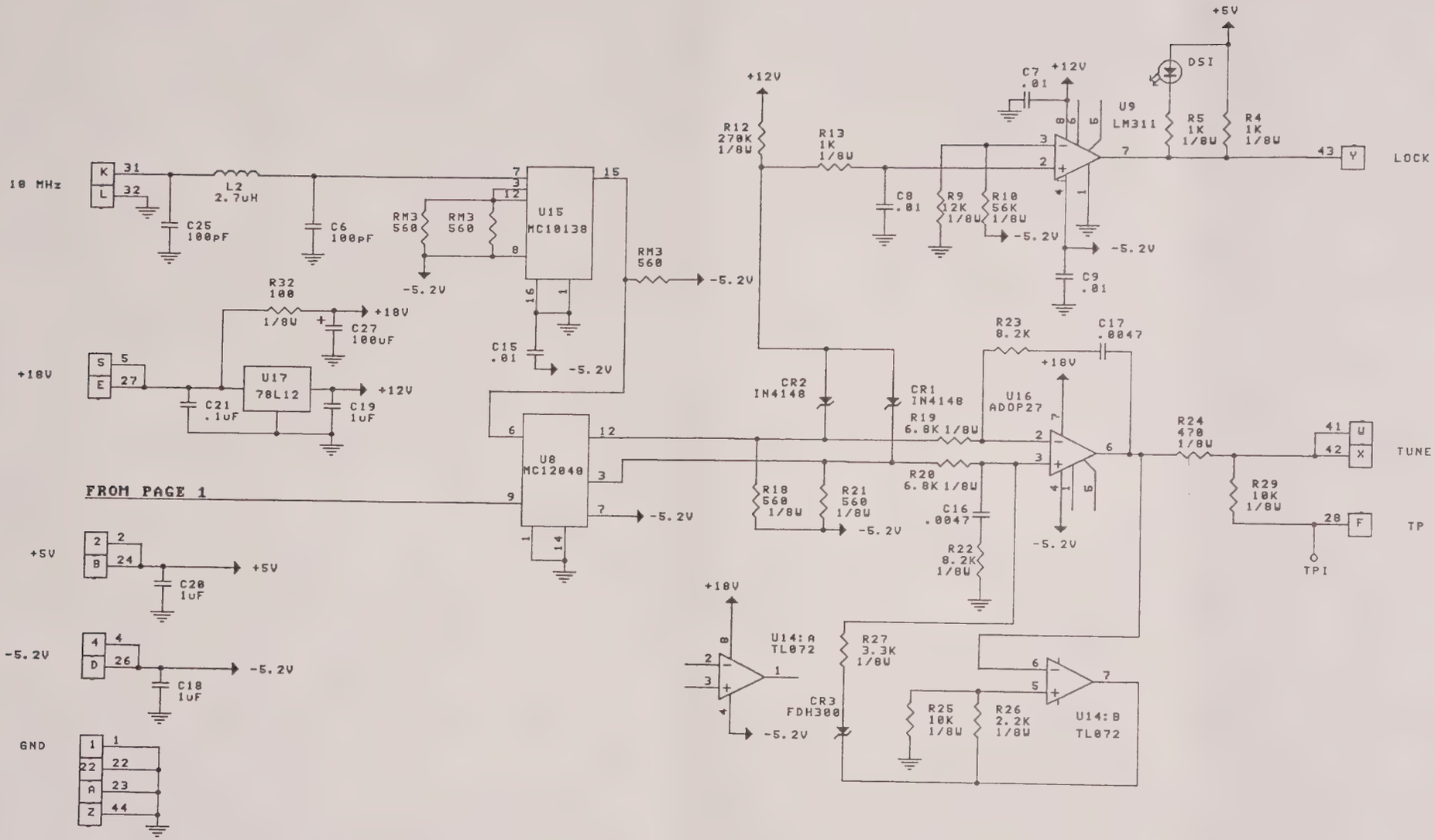
1. RESISTOR VALUES ARE IN OHMS
2. CAPACITOR VALUES ARE IN uF
3. DIODES ARE IN4148
4. * INDICATES CHIP CAP

300 MHz Phase Lock Loop (A11)

DWG# 304BM02200 Rev K

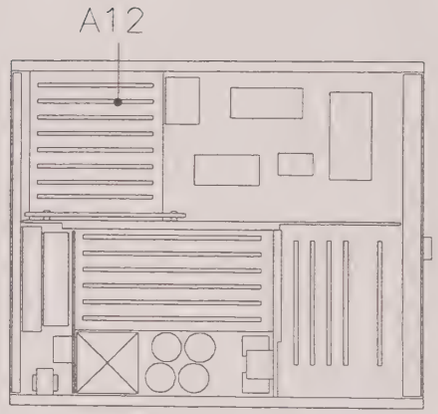
Sheet 3 of 4

7-A11-3



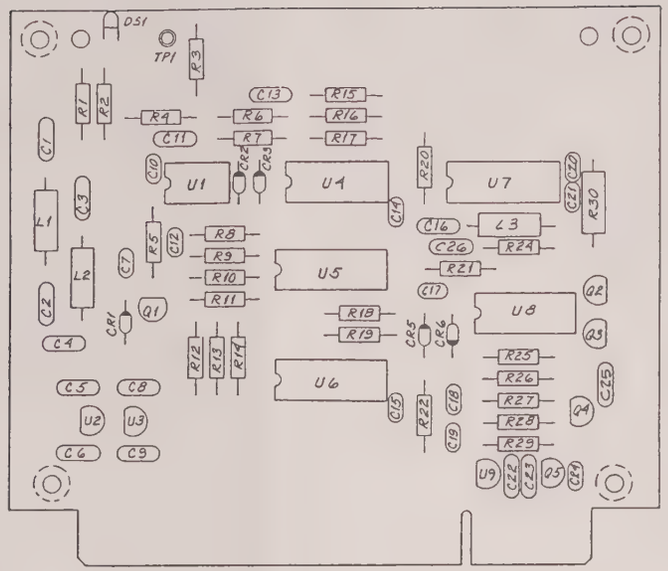
300 MHz Phase Lock Loop (A11)

DWG# 304BM02200 Rev K



110 MHz Phase Lock Loop (A12)

DWG# 304BM05600 Rev F



110 MHz Phase Lock Loop (A12)

DWG# 304BM05600 Rev F

Sheet 2 of 3

7-A12-2

110 MHz PHASE LOCK LOOP -- PC ASSY A12

The function of this circuit is to phase lock the 110 MHz VCO on the oscillator/multiplier board (A113) to the 10 MHz master reference. In addition, this circuit performs important functions related to the master reference itself.

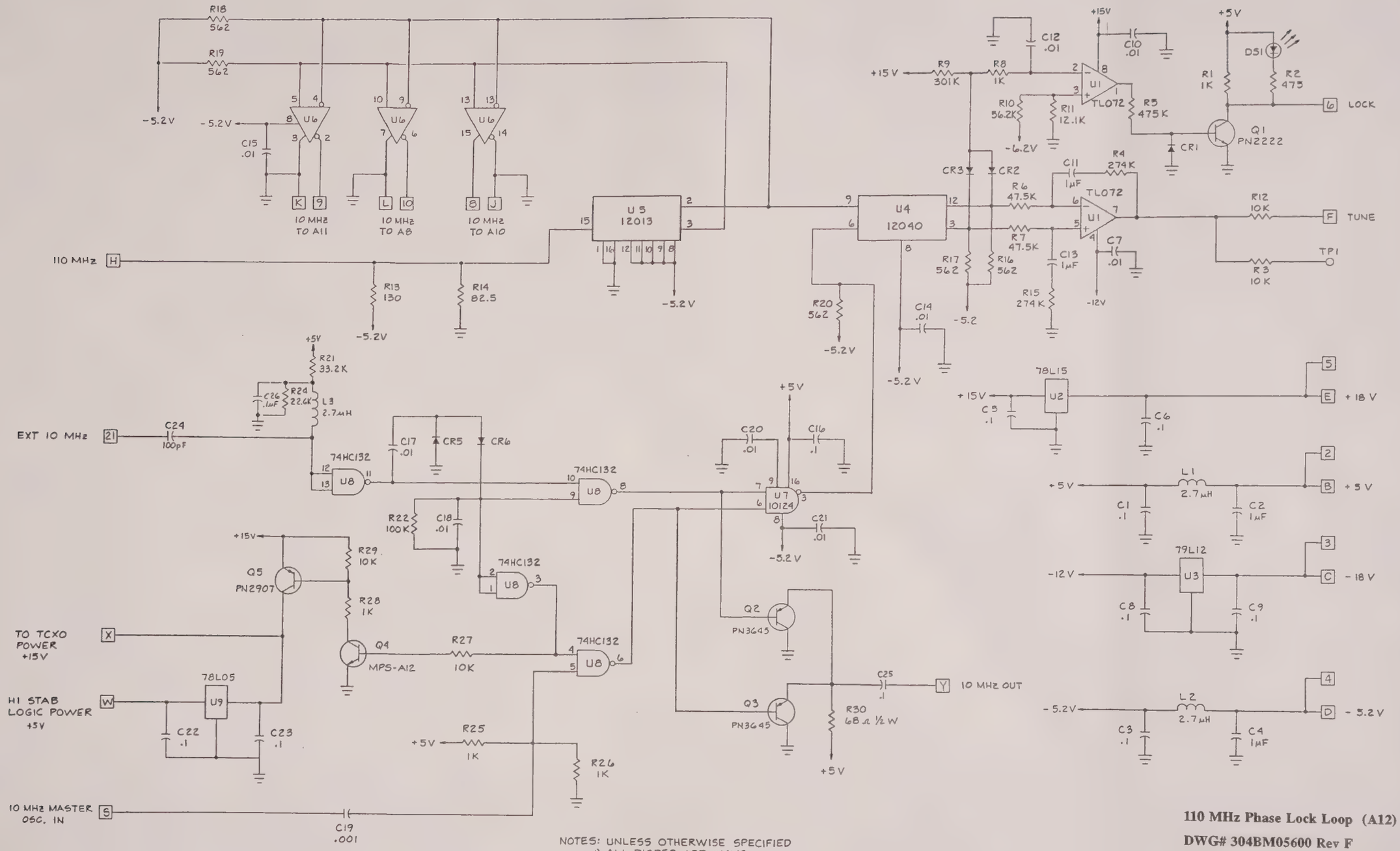
The output frequency of the 110 MHz VCO is received at pin H; U5 divides this input by 11. When the loop is locked, the input is exactly 110 MHz, and the divider's output is exactly 10 MHz. This output is applied to the variable input of the phase comparator at U4-9. The reference input to the phase comparator comes from the 10 MHz input/output circuit.

The instrument is designed to accept an external 10 MHz timebase input, and this external input, whenever present, is automatically substituted for the internal timebase. The external 10 MHz signal is received at pin 21; the input is AC coupled (C24); U8-11 is triggered by an input of 1 Vpp or greater. When an external input is present, the signal propagates through U8-8 and TTL-ECL translater U7-3 to the reference input of the phase detector at U4-6. The external signal is also used to charge C18, so that U8-3 is held low. This low level turns off Q4 and Q5, cutting off the +15V and +5V power supplies to the internal timebase oscillator, so that it will not interfere with the external timebase. The timebase signal also propagates through Q2 to the instrument's timebase output, via pin Y.

When no external 10 MHz input is present, U8-3 is held high; Q4 and Q5 are turned on and the supply voltages are furnished to the internal timebase oscillator. The input from the internal timebase, received at pin S, propagates through U8-6 and U7-3 to the phase detector. The timebase signal also propagates through Q3 to the instrument's timebase output, via pin Y.

When its reference and variable inputs are not in phase, U4 produces wide pulses at one of its outputs, depending on whether the variable input is leading or lagging the reference. The pulsed outputs are filtered and amplified by U1-7 to produce a voltage output (pin F) which tunes the 110 MHz VCO.

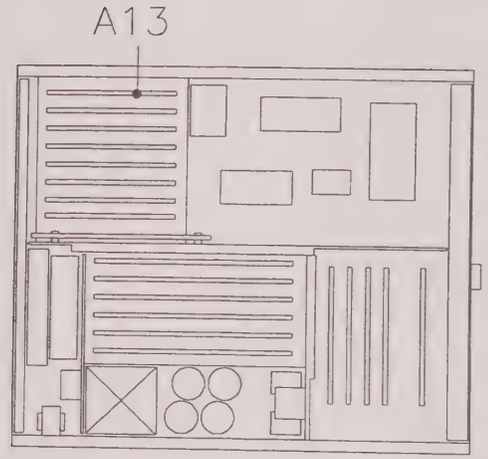
The lock indicator circuit (U1-1, Q1) responds to the wide pulses which occur on the phase detector outputs when the loop is unlocked by turning on Q1, pulling the output low, and illuminating DS1. When the loop is locked, Q1 is off and DS1 is dark.



NOTES: UNLESS OTHERWISE SPECIFIED
1) ALL DIODES ARE IN4148
2) CAPS ARE IN µF
3) RESISTORS ARE IN OHMS

110 MHz Phase Lock Loop (A12)

DWG# 304BM05600 Rev F

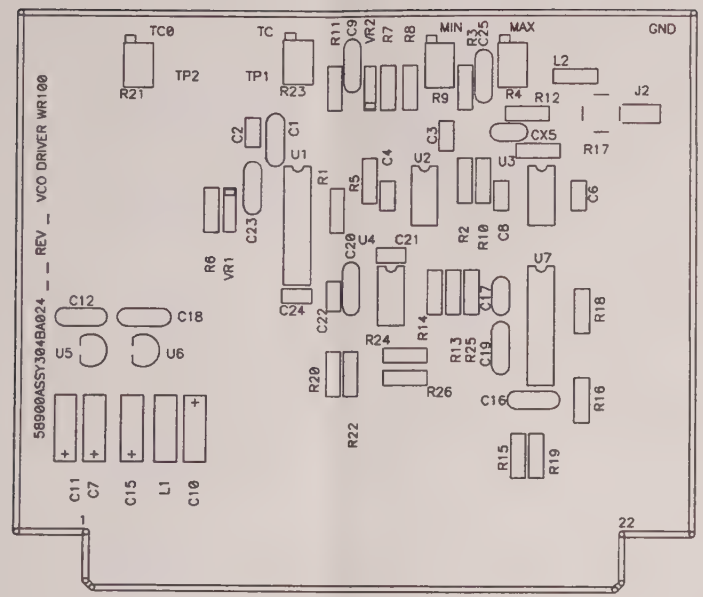


VCO Driver (A13)

DWG# 304BM02403 Rev A

Sheet 1 of 3

7-A13-1



VCO DRIVER -- PC ASSY A13

The function of this circuit is to tune the instrument's RF output VCO. This single tuning output is a composite of various tuning and correction signals.

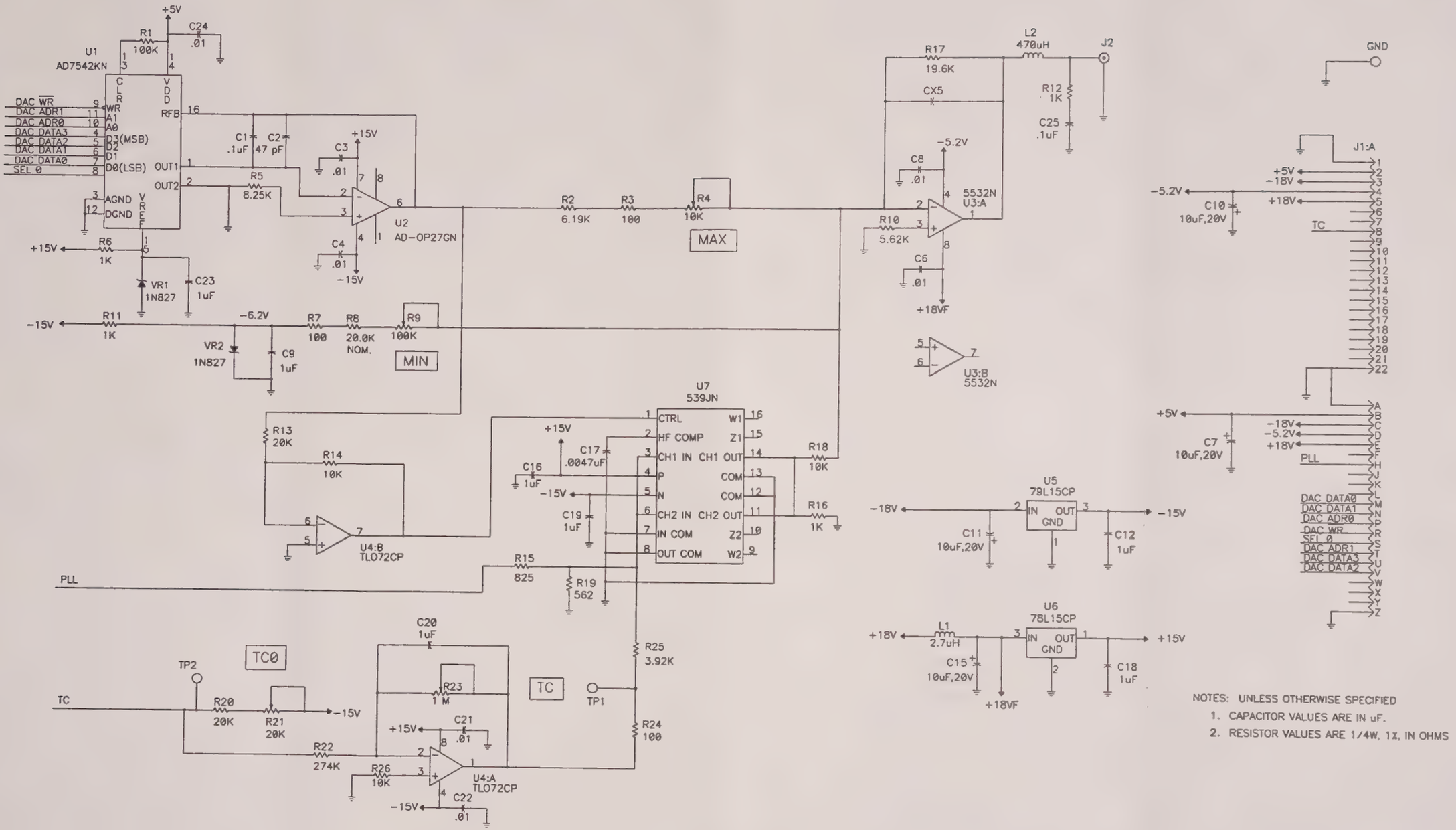
U1, a multiplying DAC, generates the basic tuning voltage for the VCO. Its output is based on a reference voltage (+6.2V) regulated by VR1. This voltage is multiplied by a factor which is programmed by the computer to achieve the desired output frequency. The tuning voltage is amplified and inverted by U2 and furnished to the summing junction of the output amplifier (U3-2). R4 and R9, the MAX and MIN pots, allow for calibration of the output at the extremes of the VCO's frequency range.

The VCO is a nonlinear device; its tuning sensitivity varies for different parts of its frequency range. In programming the DAC, the computer takes this nonlinearity into account. However, other elements of the composite tuning output must be corrected for VCO nonlinearity.

The other inputs to the summing junction of U3A are provided through U7, a multiple-input voltage multiplier. The control input to the multiplier comes from U2, by way of the buffer amplifier U4B. The basic tuning voltage from U2-6 is used as the control voltage, so that it serves as a correction factor for VCO nonlinearity. The typical range of this tuning voltage is -1.5V (fMIN) to -6V (fMAX). The inputs to U7 come from the Output PLL circuit, A6 (this input includes both phase correction and frequency modulation, if applicable), and from the temperature compensation resistor on the VCO board. Both these inputs are combined at U7-3.

Temperature compensation is needed because the frequency of the VCO varies inversely with temperature. The resistance of the temperature compensation resistor on the VCO board decreases as temperature increases, with the result that the input voltage at TP2 rises as the temperature rises. This is inverted and amplified by U4A; the output to U7-3 is a voltage which decreases as temperature increases (the voltage at TP1 will be close to zero volts at room temperature).

The phase correction, frequency modulation, and temperature compensation inputs are combined with the DAC's basic tuning voltage at the summing junction of the output amplifier (U3A, an inverting amplifier) and furnished (through J2) to the VCO board. The typical output tuning range is roughly +5V (fMIN) to +14V (fMAX).

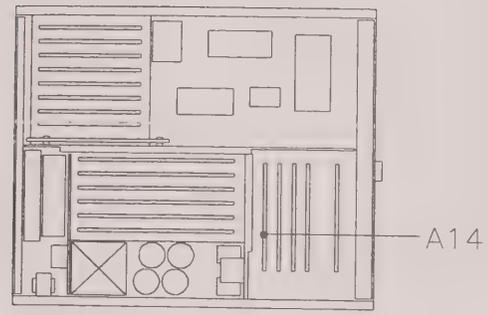


VCO Driver (A13)

DWG# 304BM02403 Rev A

Sheet 3 of 3

7-A13-3

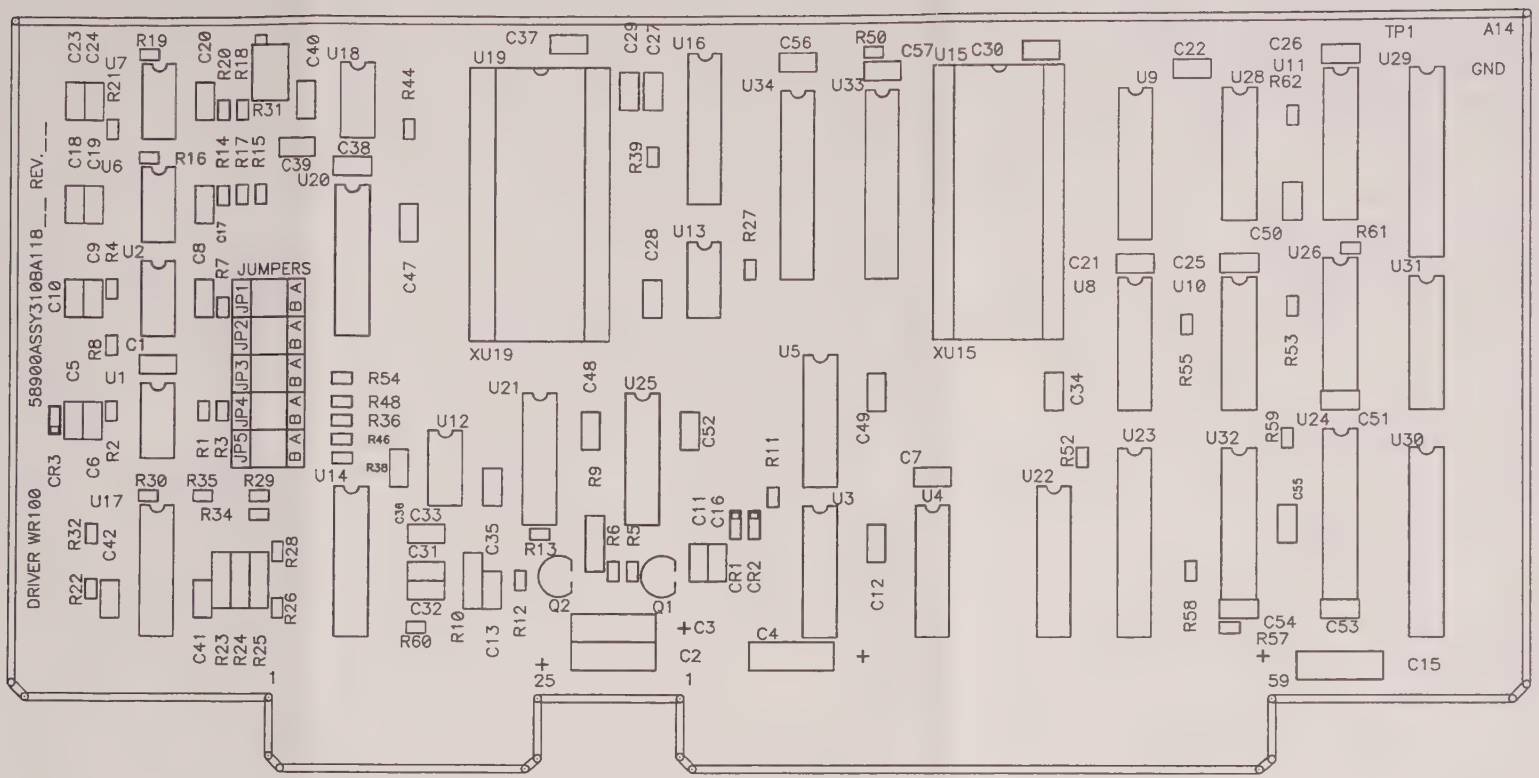


Driver (A14)

DWG# 310BM11801 Rev A

Sheet 1 of 5

7-A14-1



DRIVER -- PC ASSY A14

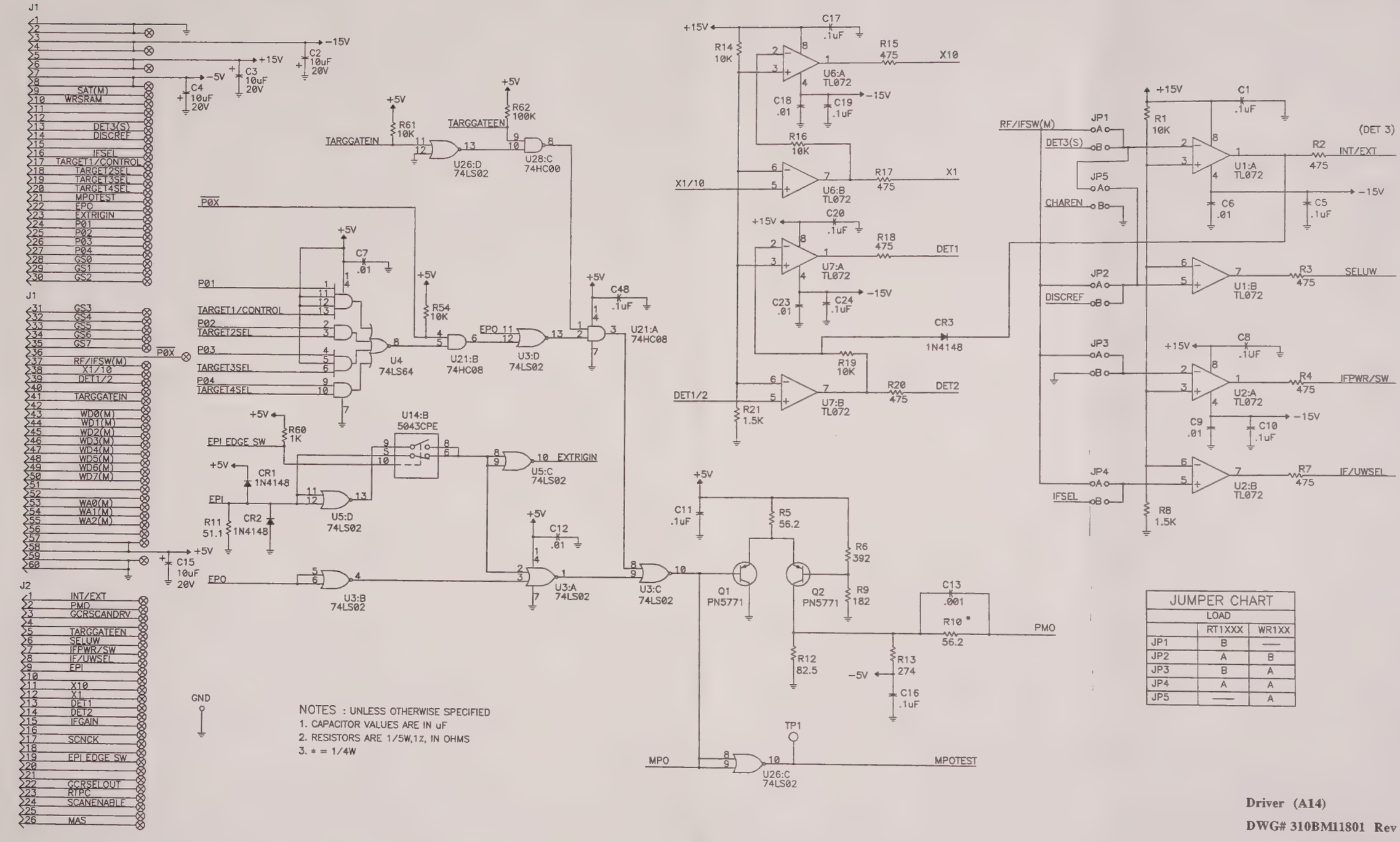
The Driver PC Assembly provides drive signals to various RF modules. The circuit is divided into four sections, having to do with switching, pulse modulation, pulse amplitude, and scan modulation.

The switching section consists of operational amplifiers U1, U2, U6, and U7. These amplifiers provide the drive current to switching diodes within the RF modules, which are used to activate detector paths and RF paths appropriate to the current operating mode.

The pulse modulation section consists of an analog drive circuit (Q1, Q2) for the pulse modulator; this is triggered by TTL signals from the multiple target combiner circuit (U4) and logic gates associated with the external pulse modulation input (U3, U5, etc). The multi-target and external signals are switched in and out by the 'EPO' line (see U3-6). When the multi-target signal is switched in, TTL pulses generated by the multi-target digital pulse generator (A15) are fed to the pulse modulator analog driver (see U3-10). When the external signal is switched in, the pulse modulator analog driver is driven from TTL pulses which are applied to the instrument from an external source.

The pulse amplitude section is shown on sheet 4 of this diagram. U22 is the master clocking circuit for the pulse amplitude section. It takes the falling edge of the TTL signal used to feed the pulse modulator and selects the appropriate memory address within U24, a static RAM programmed with target amplitude data. The data is combined with scintillation data and is subsequently fed to the scan modulation section.

The scan modulation section is a dual DAC linearized driver. The level data from the pulse amplitude section is fed to two Eproms (U15 and U19) which contains the compensation data for the scan module. The TTL compensation data is then converted by DACs U16 and U20 into an analog voltage signal, which is amplified by U12 and furnished to U17, a voltage-to-current amplifier which drives the scan module in order to control pulse amplitude.



NOTES : UNLESS OTHERWISE SPECIFIED
1. CAPACITOR VALUES ARE IN uF
2. RESISTORS ARE 1/5W,1%, IN OHMS
3. * = 1/4W

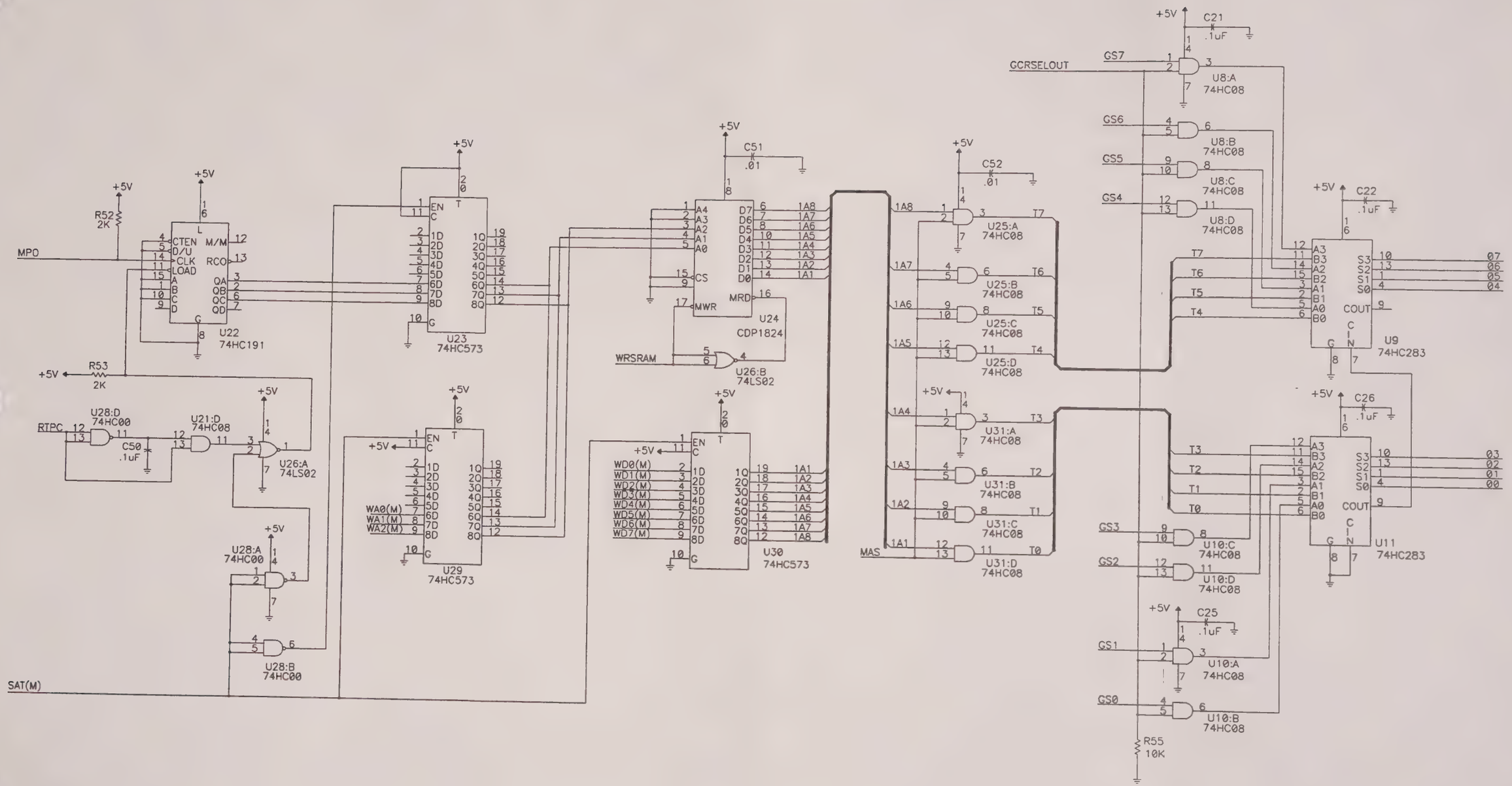
JUMPER CHART		
	LOAD	
	RT1XXX	WR1XX
JP1	B	—
JP2	A	B
JP3	B	A
JP4	A	A
JP5	—	A

Driver (A14)

DWG# 310BM11801 Rev A

Sheet 3 of 5

7-A14-3

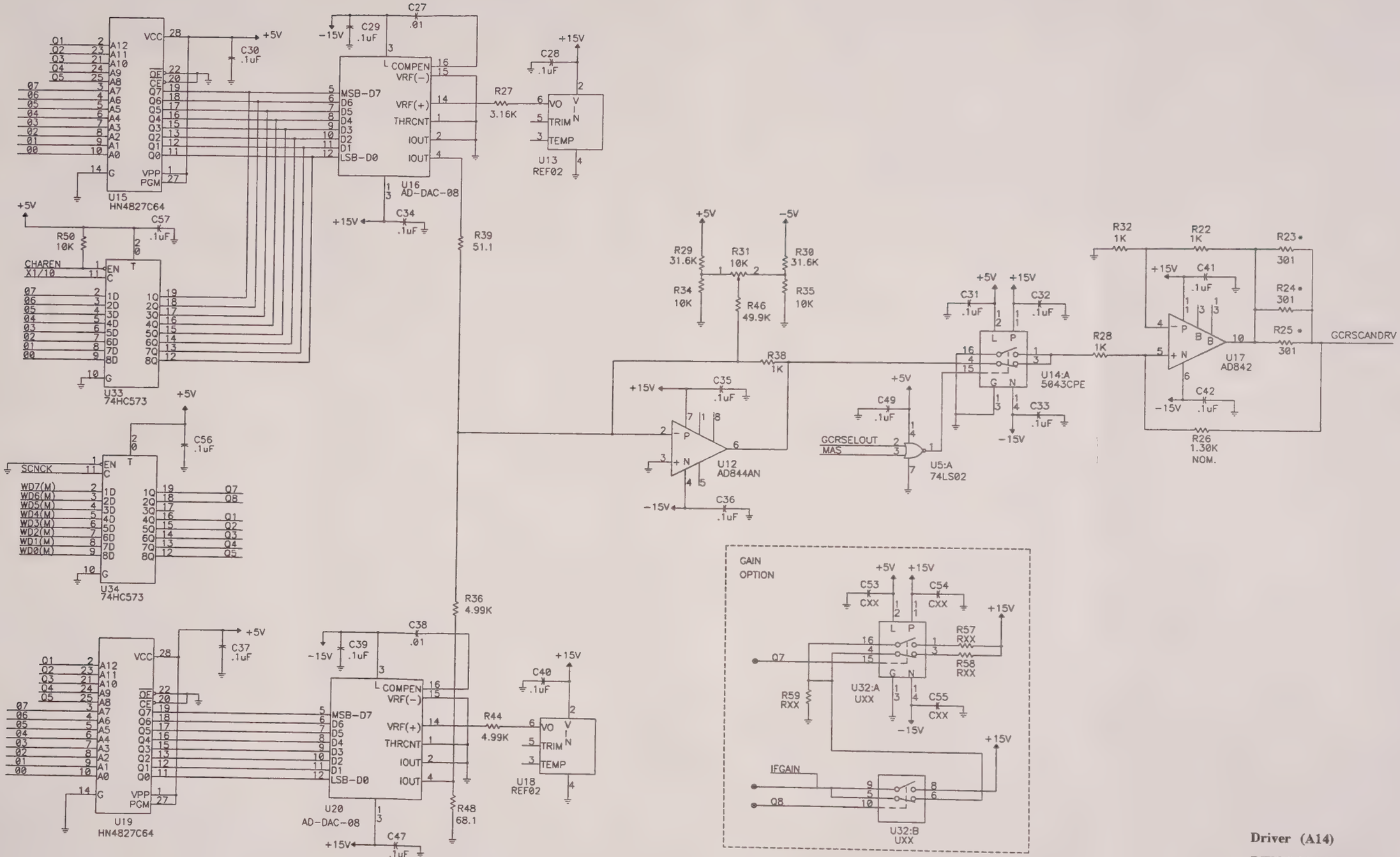


Driver (A14)

DWG# 310BM11801 Rev A

Sheet 4 of 5

7-A14-4

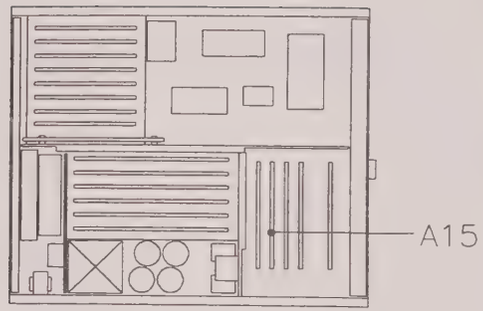


Driver (A14)

DWG# 310BM11801 Rev A

Sheet 5 of 5

7-A14-5

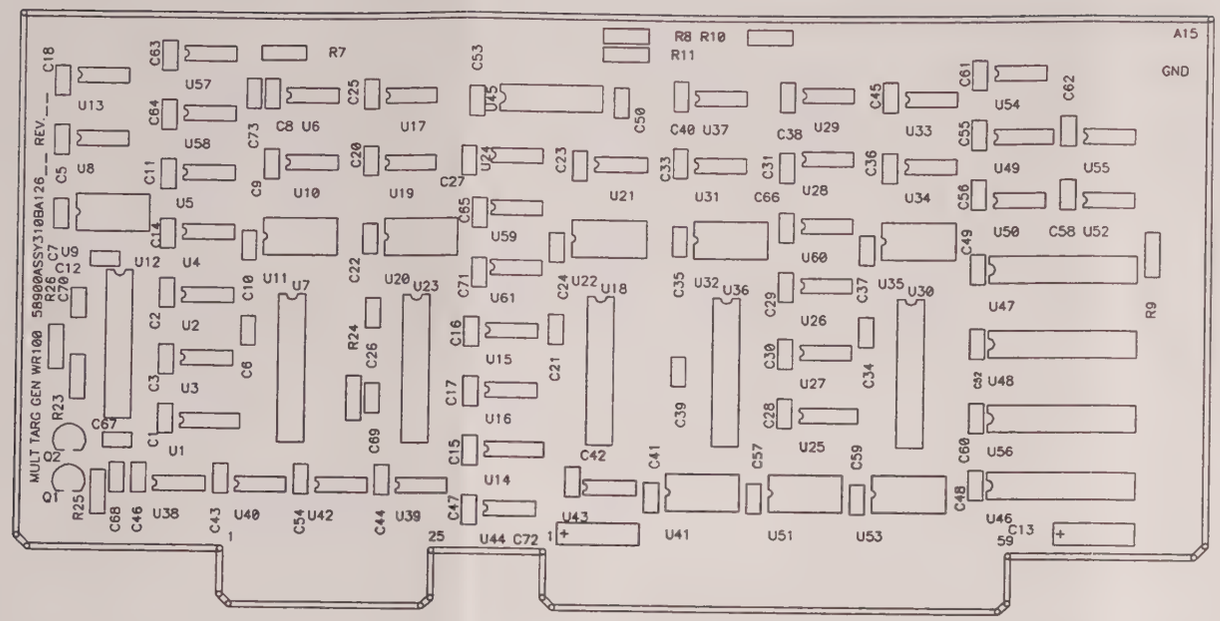


Multi Target Generator (A15)

DWG# 310BM12600 Rev B

Sheet 1 of 6

7-A15-1



MULTI-TARGET GENERATOR -- PC ASSY A15

This circuit derives timing intervals from the instrument's timebase oscillator in order to control pulse rate, width, and delay functions.

The pulse rate is produced by oscillator U45 and controlled by phase lock loop U46 (see sheet 6). U46 contains latches to store the values for both the reference and the variable dividers; therefore it is programmed directly from the computer 'WD' lines. A second PLL chip (U47) provides programmable division of the rate generator. Both the reference and the variable dividers are used to give the wide range required. The phase detector portion of the IC is not used. Again, the internal latches allow direct programming by the computer. Secondary strobe decoder U49:A supplies timing strobes for both U46 and U47. Latch U41 is used to select the 'source' for the pulse rate. The various outputs function as follows:

U41-19 enables Target 1
U41-18 enables Target 2
U41-16 selects faster pulse rates
U41-15 selects slower pulse rates
U41-14 selects external trigger operation
U41-13 enables Target 3
U41-12 enables Target 4

The various gates of U43, using the outputs of U41, select the appropriate signal as the main pulse rate. The TARGET1/CONTROL signal is used to gate the 10 MHz timebase signal via U39:A.

To determine the start of the pulse, the rate signal is synchronized to the 10 MHz timebase by U40:A, shaped into a narrow pulse by U33:D-F and U2:B, and delayed by U27:C, U42:B, and U38:D-E. The resulting signal, Pulse/Gen/Trig, sets the flip-flop U37:B for Target 1, which in turn furnishes the 10 MHz to the delay timer circuit via U39:D. The Pulse/Gen/Trig also sets flip-flops U4:B (see sheet 3) for Target 2, U13:A (see sheet 4) for Target 3, and U28:A (see sheet 5) for Target 4. Each of these flip-flops furnishes the 10 MHz reference to the appropriate delay timer circuits. The delay circuits are similar for all targets; the delay circuit for Target 1 is described below.

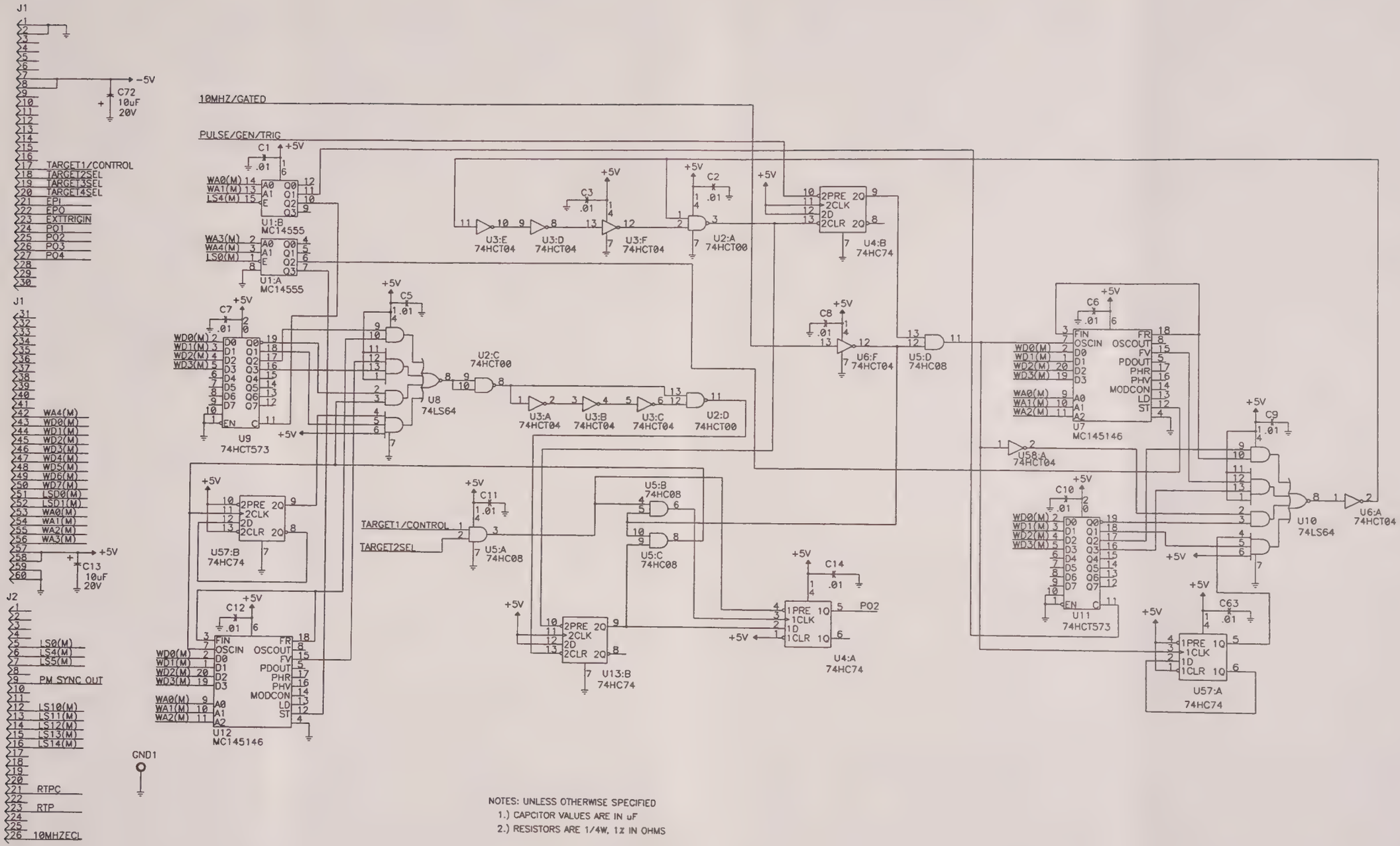
The delay timing circuit consists of a phase lock loop IC used as a dual programmable counter (U48 for Target 1), a divide- by-two (U40:B for Target 1), a control latch (U51 for Target 1), and gates (U50 for Target 1) to select the desired delay source. The outputs of U51 function as follows:

Q0: fixed .1 us delay
Q1: fixed .2 us delay
Q2: short variable delay
Q3: long variable delay

For Target 1, to produce the shortest delay, .1 uS, the output of U39:D is routed directly through the gating circuit. The pulse start signal from U50 occurs .1 uS after the rate trigger at U40:A. For a .2 uS delay, divider flip-flop U40:B is activated and selected. These two fixed delays are required since the programmable divider has a lower divide limit of 3. Delays greater than .2 uS are provided by U48; either one or both U48 internal programmable dividers are used, depending on the amount of delay required.

For Target 1, the pulse start signal from U50 is shaped into a narrow pulse by U33:C, U42:D-E, and U44:A, and enables the pulse out via U54:A. U55:A, once enabled by U54:A, will be clocked by the 10 MHz and start the pulse.

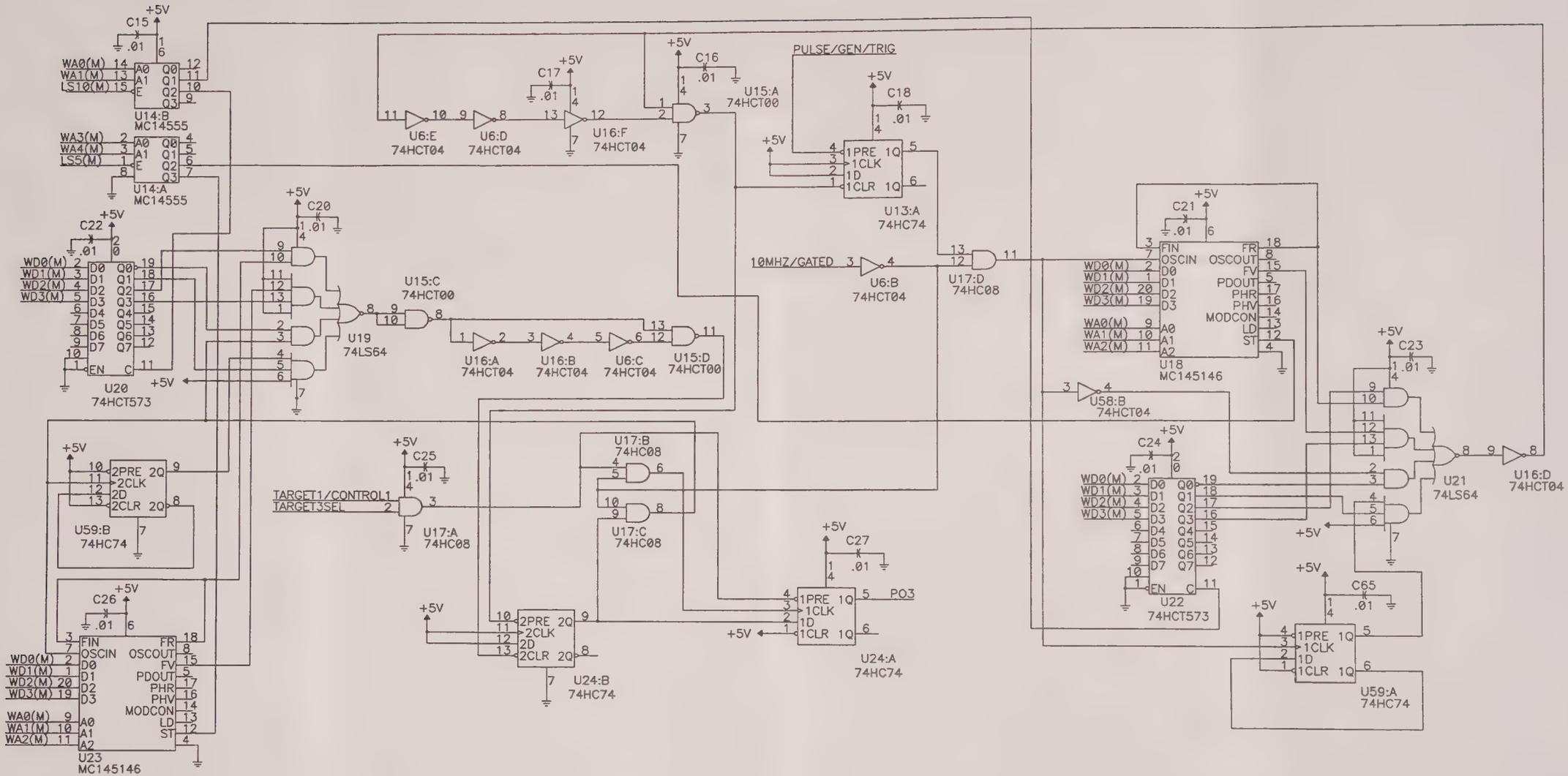
A circuit identical in function to the delay generator (see U53, U52) is used to determine the width of the pulse. The clock for the circuit begins after the delay interval via U39:C. The pulse forming network, U42:A, U42:C, U38:C, and U44:D, supplies the 'stop' signal to U54:A, which then ends the pulse. A similar width generator circuit is used for each of the other targets.



NOTES: UNLESS OTHERWISE SPECIFIED
1.) CAPCITOR VALUES ARE IN uF
2.) RESISTORS ARE 1/4W, 1% IN OHMS

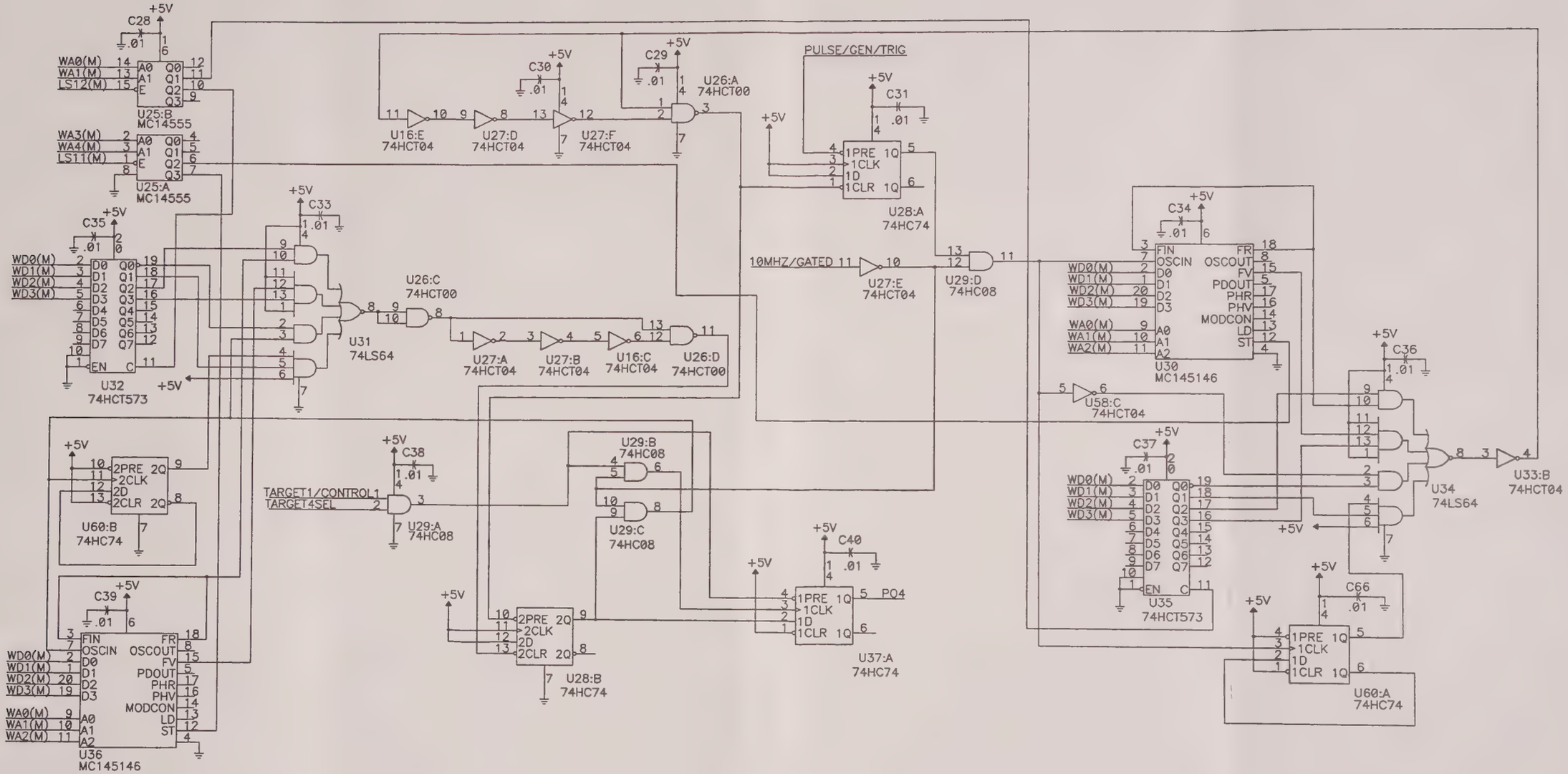
Multi Target Generator (A15)

DWG# 310BM12600 Rev B



Multi Target Generator (A15)

DWG# 310BM12600 Rev B

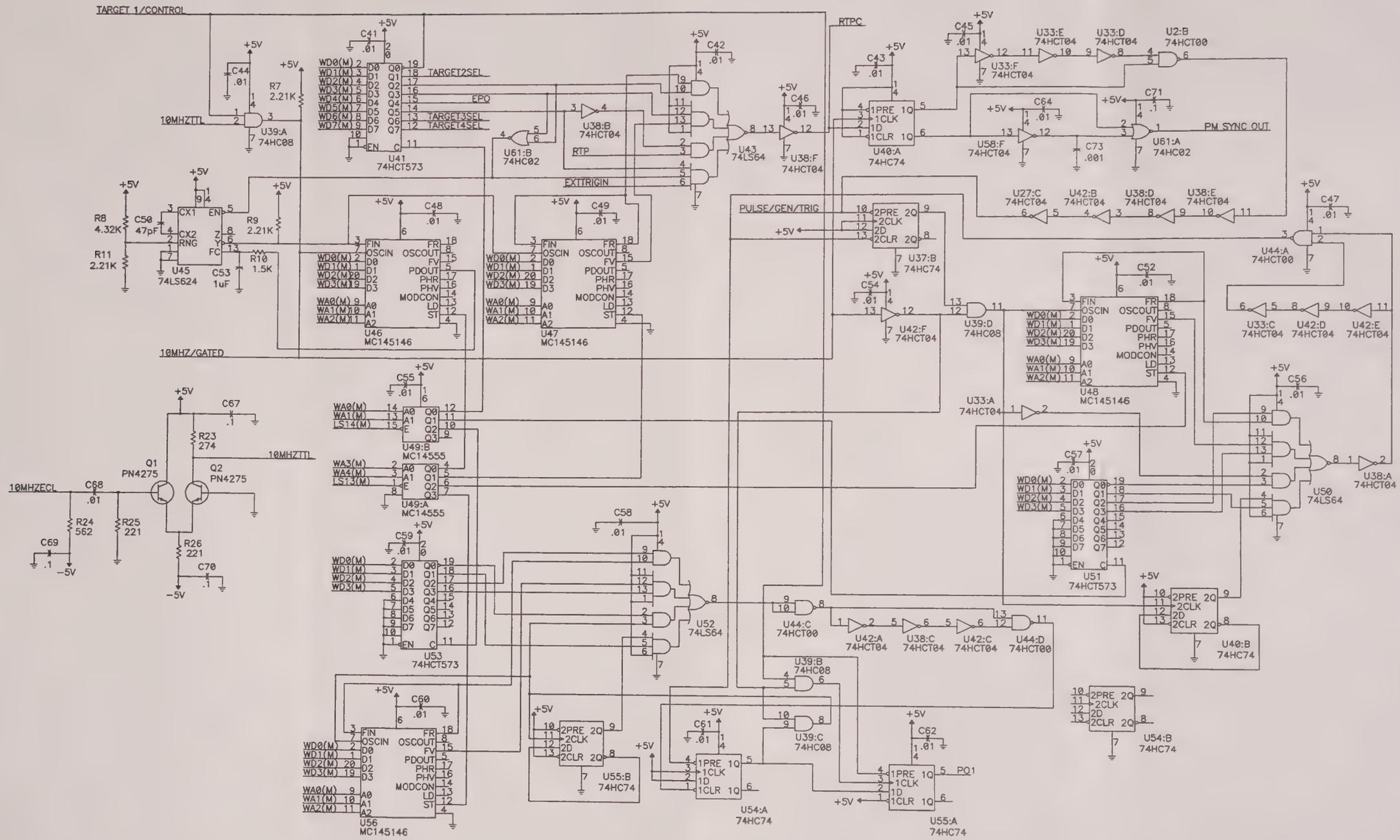


Multi Target Generator (A15)

DWG# 310BM12600 Rev B

Sheet 5 of 6

7-A15-5

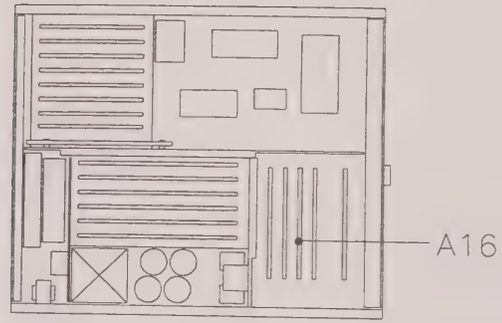


Multi Target Generator (A15)

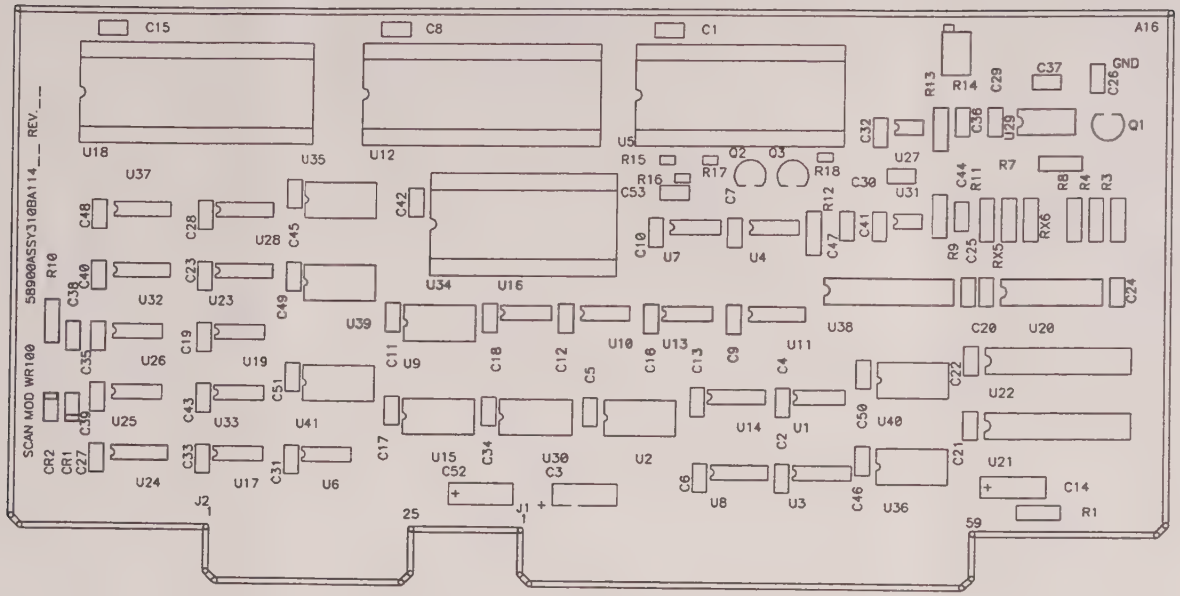
DWG# 310BM12600 Rev B

Sheet 6 of 6

7-A15-6



Scan Modulation (A16)
DWG# 310BM11400 Rev C
Sheet 1 of 4
7-A16-1



SCAN MODULATION -- PC ASSY A16

This board houses the circuits which provide input to the scan modulator, for all three scintillation modes (Turbulence 1, Turbulence 2, and STC).

Scintillation patterns are stored in EPROMs. U5, an 8K by 8 EPROM, holds up to 32 STC patterns in different memory sectors. The computer selects the memory sector by addressing the EPROM's high-order address lines by way of latch U2.

U12, a 128K by 8 EPROM, holds up to eight Turb2 patterns. The computer selects the memory sector by way of latch U6.

U18, a 128K by 8 EPROM, holds up to Turb1 patterns. The computer selects the memory sector by way of latch U15.

The 8-bit scintillation pattern output from each EPROM must pass through a set of AND gates (U1, etc.), so that the scintillation pattern is transmitted only when the appropriate mode enable line is on. In addition, the Turb1 output from U18 must pass through an additional circuit (see sheet 4) which controls modulation depth.

The scintillation pattern outputs for all three modes are summed by the TTL adders U11, U14, U3, and U8. If a particular mode is disabled, its pattern output is set to all zeroes, so that it has no effect on the sum. The summed scintillation patterns are furnished to the Driver PC board (A14), to be turned into a control input to the scan modulator.

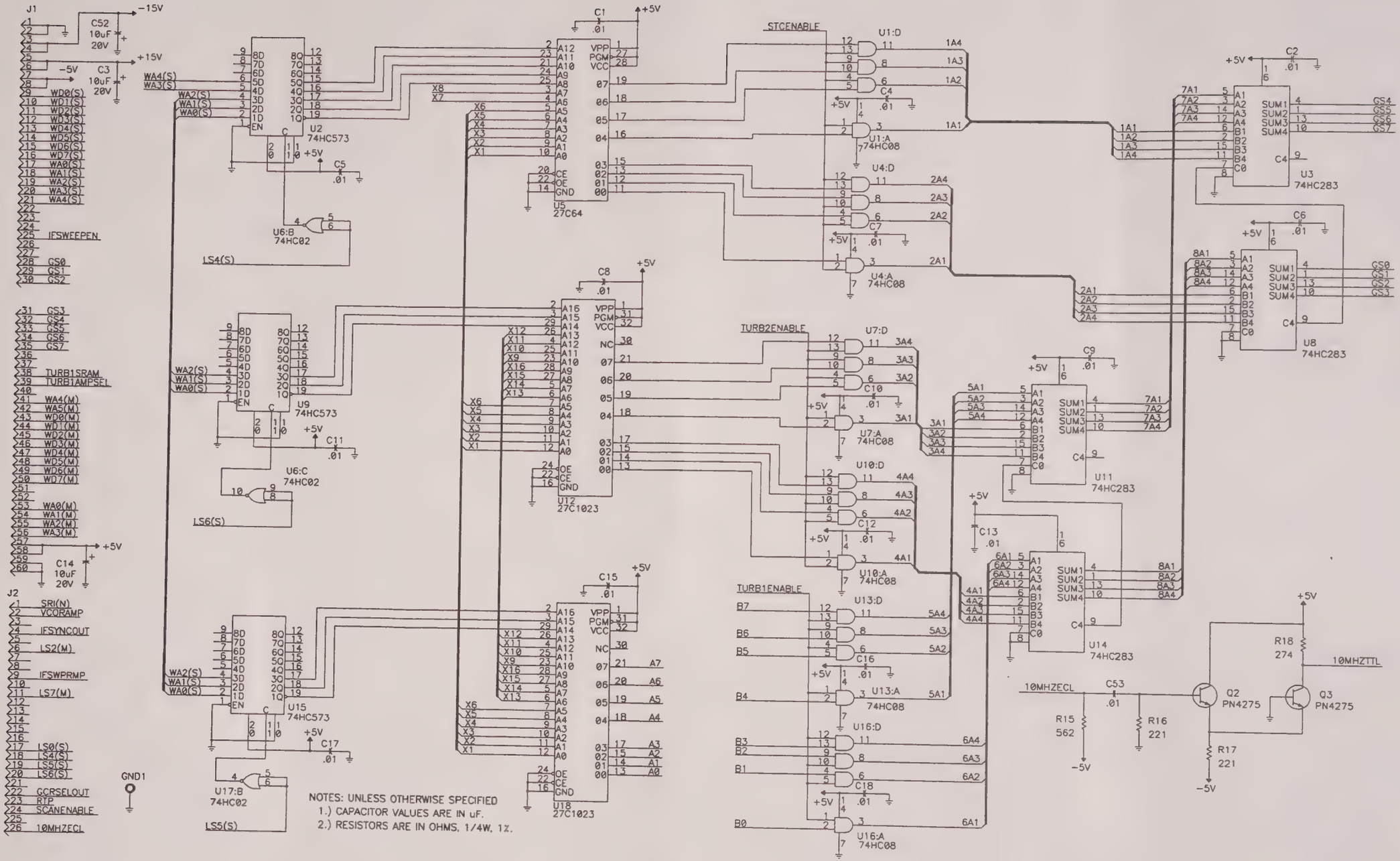
The circuit consisting of Q2 and Q3 translates a 10 MHz reference input signal from ECL to TTL levels; the TTL 10 MHz signal is used as a reference input by U21 (see sheet 4).

On sheet 4, the circuit consisting of U20, U21, U22, and U24 is a pulse generator. Its rate is programmed directly by the computer. The pulse generator runs continuously; U33-B is used to gate its output. The pulse generator output clocks the 256-step counter consisting of U23 and U28. The eight output lines of this counter are furnished to the low-order address lines of the scintillation EPROMs (see sheet 3), so that different addresses within the active memory sector are selected as the counter cycles through its 256 steps.

In addition, each 256th step of the first counter also clocks a second counter consisting of U32 and U37. The eight output lines of the second counter are furnished to the middle-order address lines of the Turb1 and Turb2 scintillation EPROMs; this allows for pattern variation with azimuth, as the scintillation pattern is read from different memory addresses during the radar sweep.

The circuit consisting of U34, U35, U39, and U40 controls the modulation depth for the Turb1 pattern. U34 is a RAM; the other three ICs are latches. The computer uses the latches to program the RAM with "ON" and "OFF" power levels for the Turb1 modulation pattern (the pattern stored in the Turb1 EEPROM, U18, indicates only the timing of the "ON" and "OFF" intervals, not their levels). The RAM output data lines (B0 through B7) are applied to the TTL adders (see sheet 3).

This board also houses a circuit which is not connected with the scan modulation function. This is the ramp generator circuit which is used in the IF Sweep mode. The oscillator circuit consisting of Q1 and U29 builds up a charge on C26 in order to produce a voltage ramp which is amplified by U27-A and U31-A. This ramp is applied to U38, a multiplying DAC. The DAC is programmed with a multiplier by the computer, through the latches U36 and U41, in order to define the slope of the ramp. The DAC output (U38-1) is amplified by U27-A and furnished to the Output PLL PC board (A6). This output is also fed back to the DAC at U38-18.

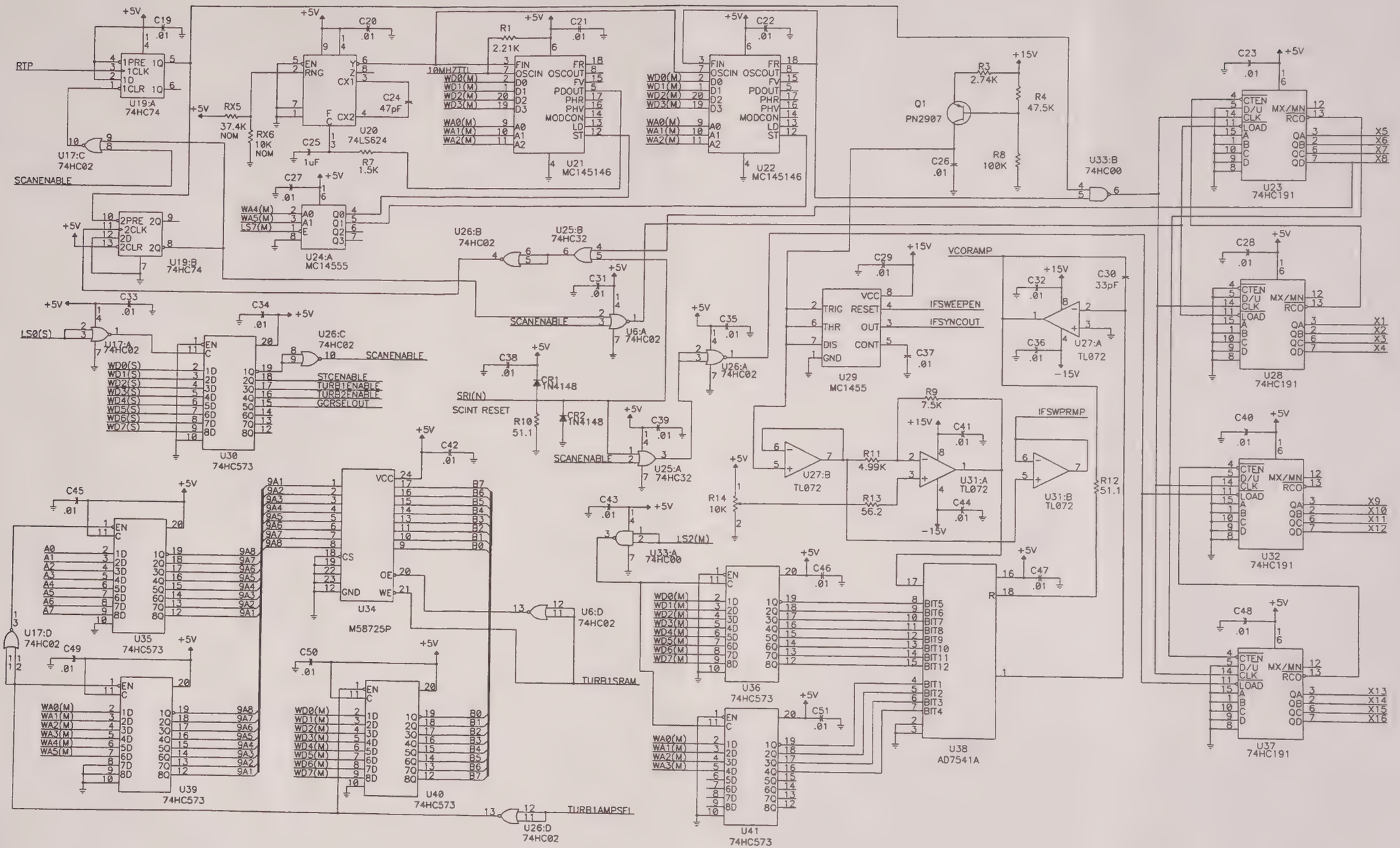


Scan Modulation (A16)

DWG# 310BM11400 Rev C

Sheet 3 of 4

7-A16-3

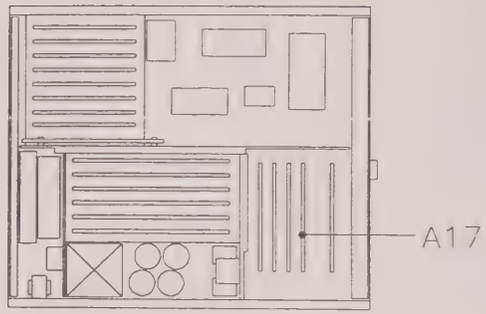


Scan Modulation (A16)

DWG# 310BM11400 Rev C

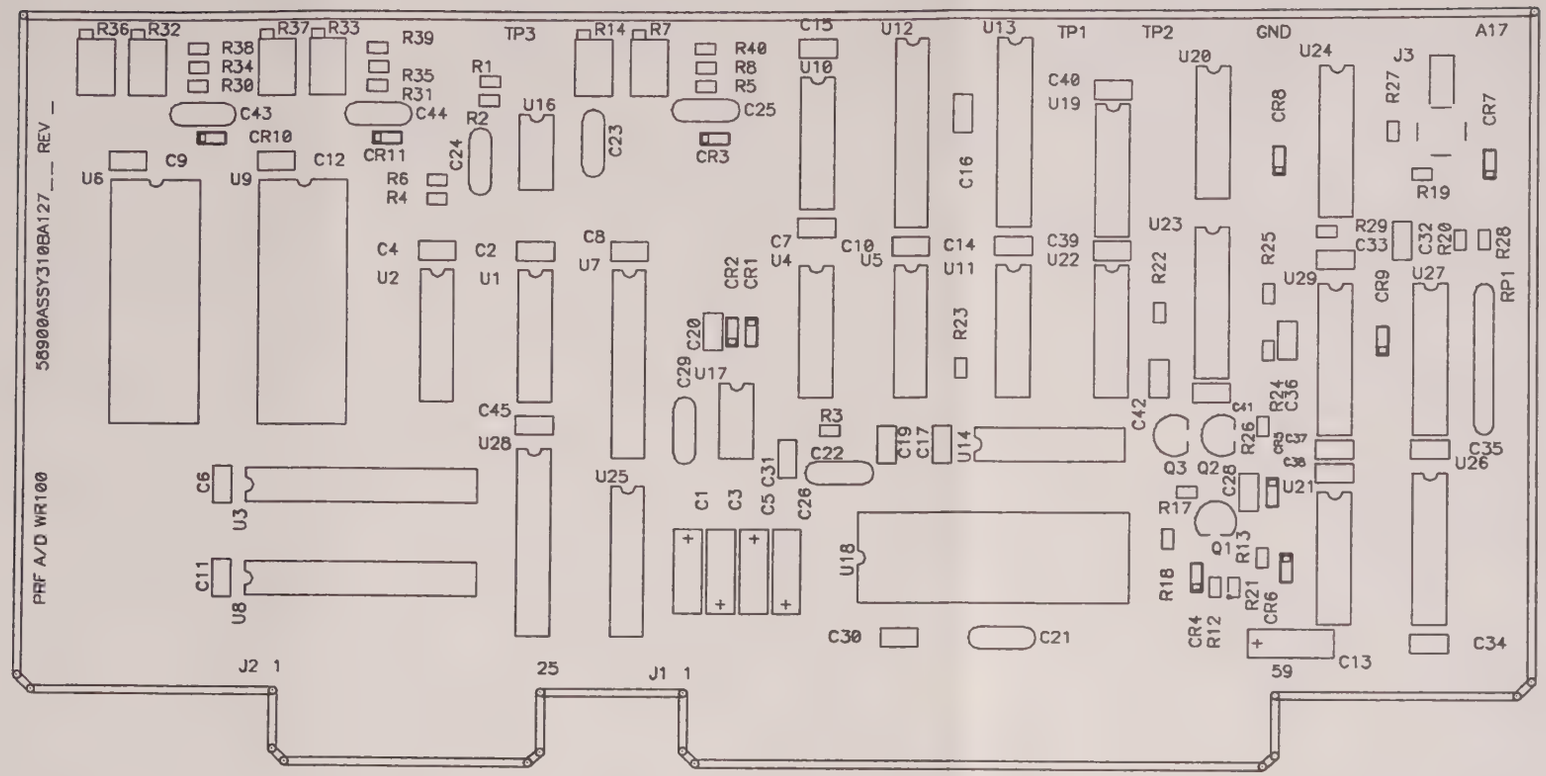
Sheet 4 of 4

7-A16-4



PRF A/D (A17)

DWG# 310BM12701 Rev 2



PRF A/D -- PC ASSY A17

The PRF A/D Peak Det Board is a multi-function board. It has three distinct sections of circuits which are used for different functions. The first section is the PRF circuitry which is used for determining the input pulse repitition frequency. The second section is the PW circuitry which is used for determining the input pulse width. The last section is the A/D Peak Det circuitry which is used for measuring input peak power.

The PRF section can be further broken down into two separate sections. These are the average and instantaneous circuits. The Average or One Second PRF is used to determine all the pulses that occur within a 1 second window. The Instantaneous PRF is used to determine the PRF rate of the pulses which occur in a transmission sequence. The Instantaneous PRF rate is a sync-PRF which means that a sync pulse (simultaneous with the first pulse within the burst train) needs to be supplied to the Rear Panel PRF/PW Sync Input.

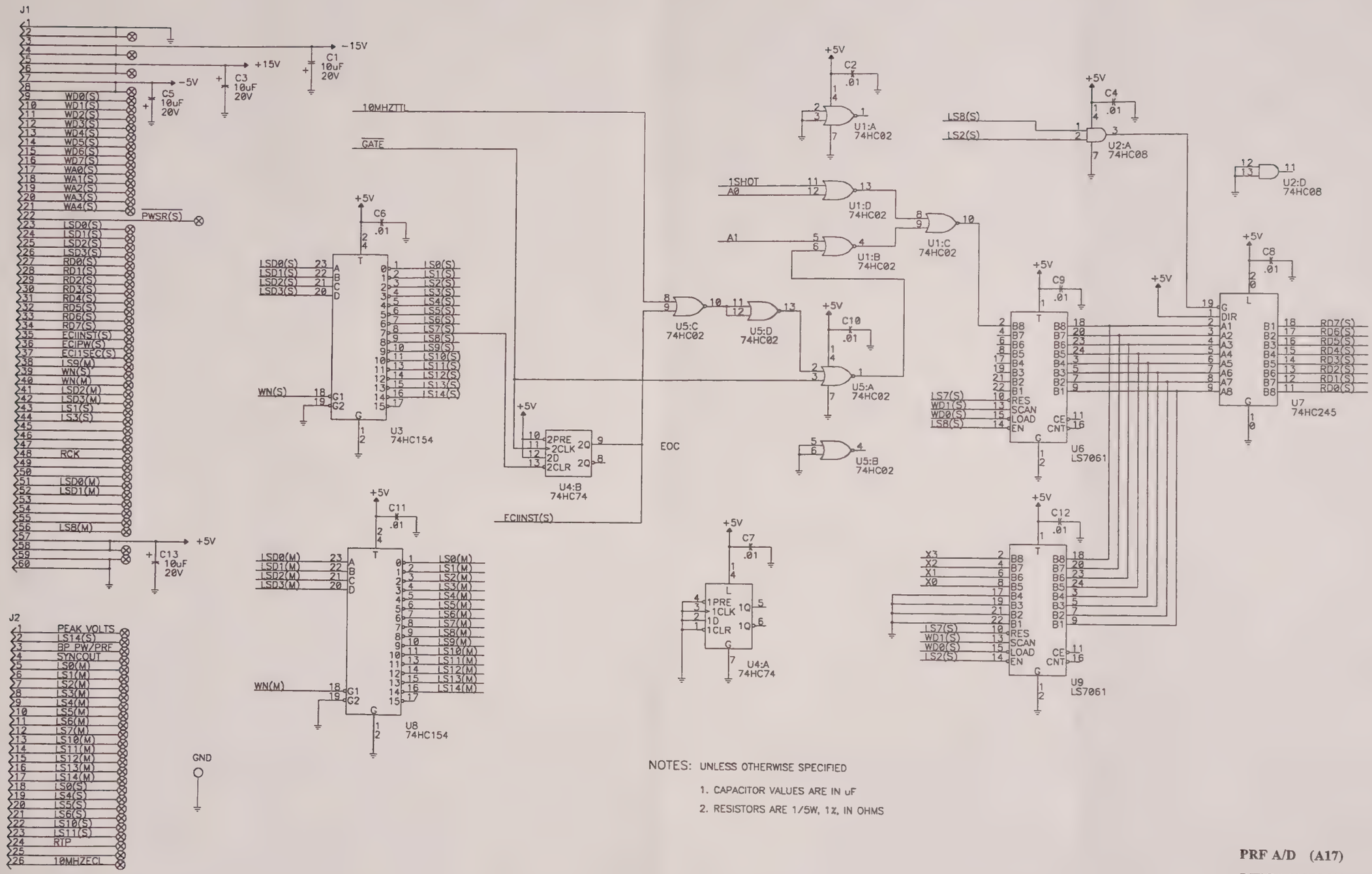
The Average or One Second PRF circuits generate a one second window using two prescalars (U12 and U13) and a flip-flop (U10:B). This window is logically ANDED with the incoming RTP by U2:B. This windowed PRF is then fed to a LS7061 via some additional control circuits. The windowed PRF count taken by the LS7061 (U6) is then fed to the computer which calculates the actual PRF rate.

The Instantaneous PRF is determined using an external TTL sync pulse from the Rear Panel coming into U21:A. This pulse is clocked through the U20:A flip-flop by the PRF which generates a sync-PRF. This sync-PRF is sent to a flip-flop U4:B and is logically 'ORed' with a 10 MHz clock signal and applied to the LS7061 (U6). U6's data is then fed to the computer which calculates the Instantaneous PRF rate.

The PW section like the preceding PRF section is also broken down into two separate sections. These are the Average and Instantaneous circuits. The Average PW is fed by the RTP signal. The RTP signal is logic gated to determine whether it is an average or instantaneous measurement. This signal is then fed to an ECL translator gate U23:A. This PW ECL signal is ANDED with a 110 MHz ECL at U24:D. The output is then fed to an ECL counter U27 and subsequently fed to ECL-TTL translator chips U26. The counted TTL signals are fed to a LS7061 counter U9 for additional higher order bit counting and transfer to the computer for the pulse width calculation.

The Instantaneous PW is determined in a similiar fashion like that of the Average PW with modifications to the input circuitry at U25. The Instantaneous PW functions similiarly like that of the Instantaneous PRF taking advantage of a sync-PRF/PW signal. This sync-PRF/PW is fed to an up counter U25 which counts the number of pulses which occur in the gate PRF/PW signal. The computer programs U25 to determine which pulse is to have its pulse width calculated. The signal is then fed to the ECL translator gate U23:A.

The A/D Peak detection circuitry located on this board only represents the digitizing portion of the circuits. The Peak Volts signal is a DC voltage originating from the Detector Buffer. It is then multiplied by a gain of two by the operational amplifier U16:A and then converted into a digital word by the AD 7582 (U18). The digital word is then sent to the computer for the final peak power calculation.

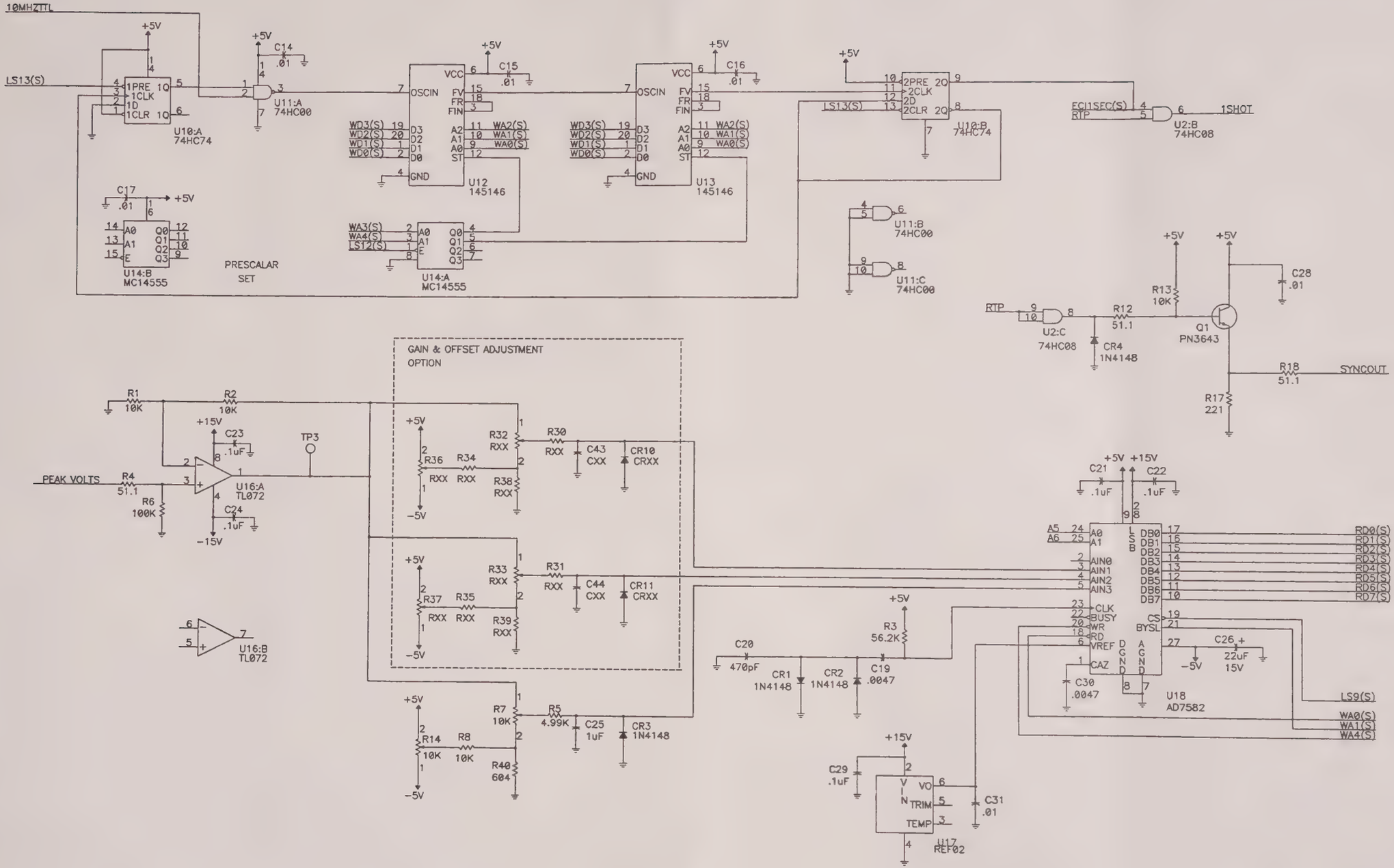


NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTORS ARE 1/5W, 1%, IN OHMS

PRF A/D (A17)

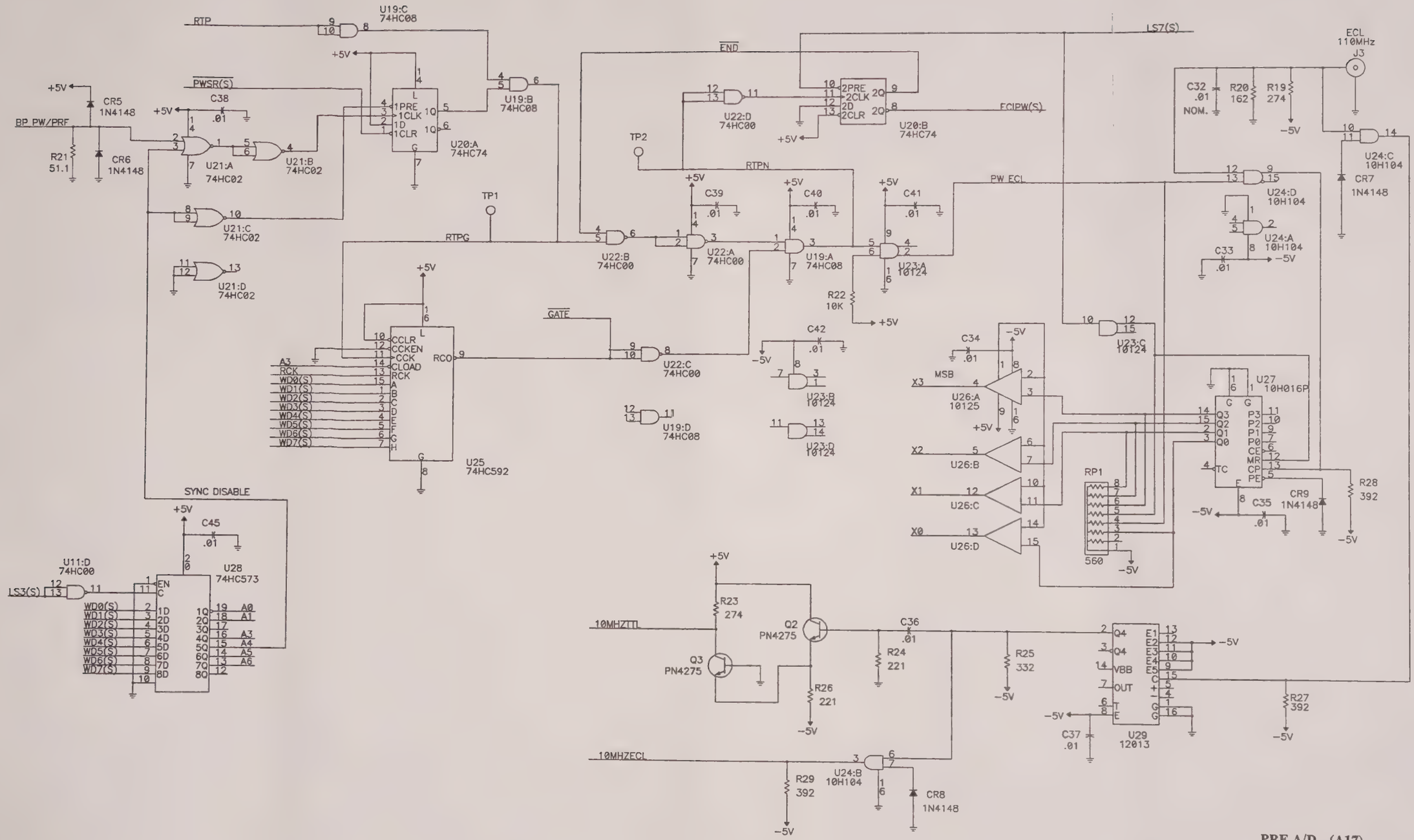
DWG# 310BM12701 Rev 2



PRF A/D (A17)

DWG# 310BM12701 Rev 2

Sheet 4 of 5

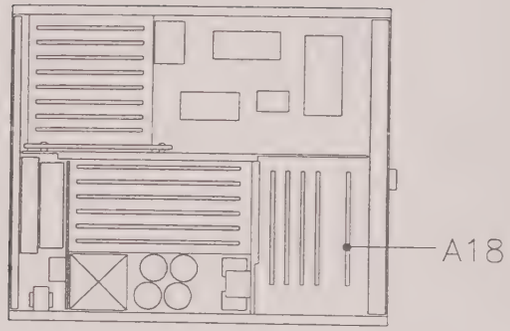


PRF A/D (A17)

DWG# 310BM12701 Rev 2

Sheet 5 of 5

7-A17-5

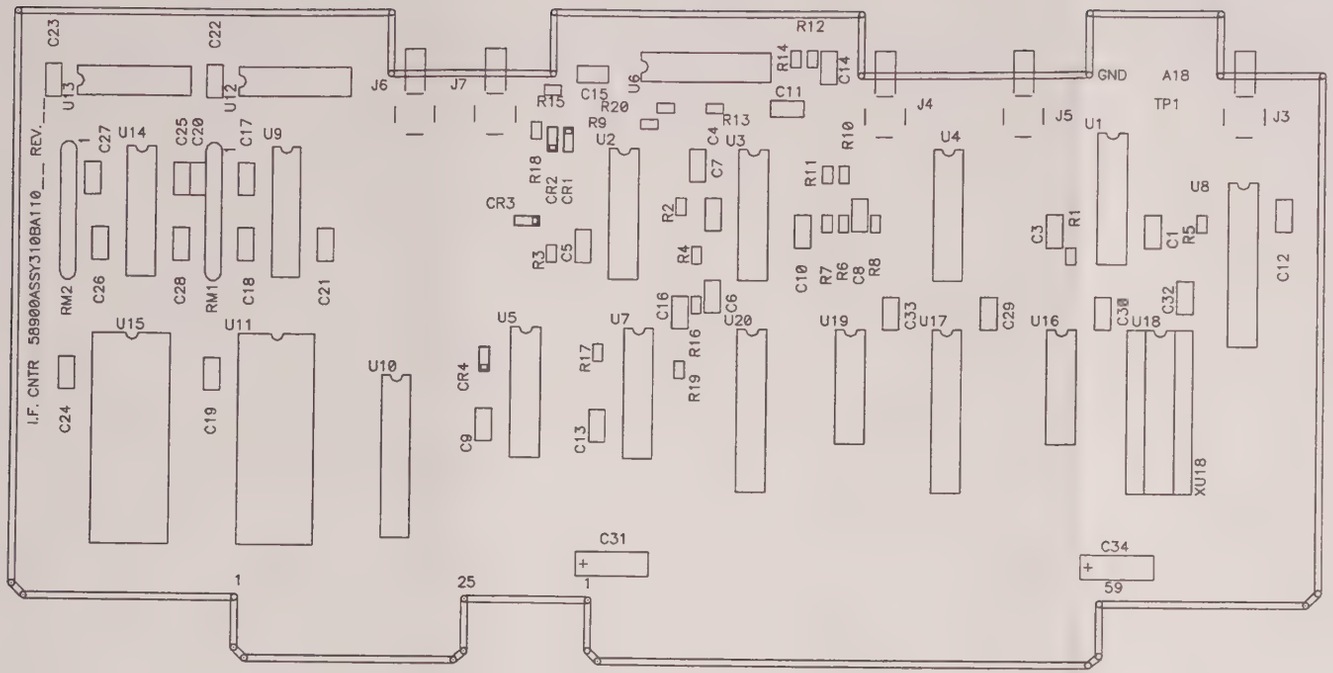


IF Counter (A18)

DWG# 310BM11001 Rev 1

Sheet 1 of 5

7-A18-1



IF Counter (A18)

DWG# 310BMI1001 Rev 1

Sheet 2 of 5

7-A18-2

IF COUNTER -- PC ASSY A18

This circuit receives and counts two frequency inputs; a fixed 110 MHz reference input at J4, and a variable I.F. input from the downconverter mixer at J7. The I.F. input has a frequency range of approximately 15 to 135 MHz. Both inputs are counted simultaneously over a fixed time period, and the ratio of counts between the two is used by the computer to determine the frequency of the I.F. input.

The TTL GATE input from the detector buffer, which indicates the presence of detected RF input, is received at J3. This input, and three control lines from the computer, are buffered by U8. The buffered gate input, which is referred to as RTP (Radar Trigger Pulse) is furnished to the Multi-Target Pulse Generator circuit board (A15) in order to coordinate the timing of input and output RF pulses.

The TTL GATE input and the ARM input (a count window, approximately 150 ms in duration, created by the computer) are logically combined by U1-B and U1-D and applied to the flip-flop U3A. The 110 MHz reference input is buffered by U4 and also applied to U3A (a second buffered 110 MHz output is furnished, via J5, to the PRF A/D Peak Detector circuit, A17). The Q1 output (U3-2) of this flip-flop controls the subsequent counter circuits, so that the frequency counter operates only when the ARM, TTL GATE, and 110 MHz inputs are in the active state.

The I.F. input at J7 is buffered by U6 and applied to U3B (a second buffered IF output is furnished, at J6, to the Discriminator Amplifier circuit, A114).

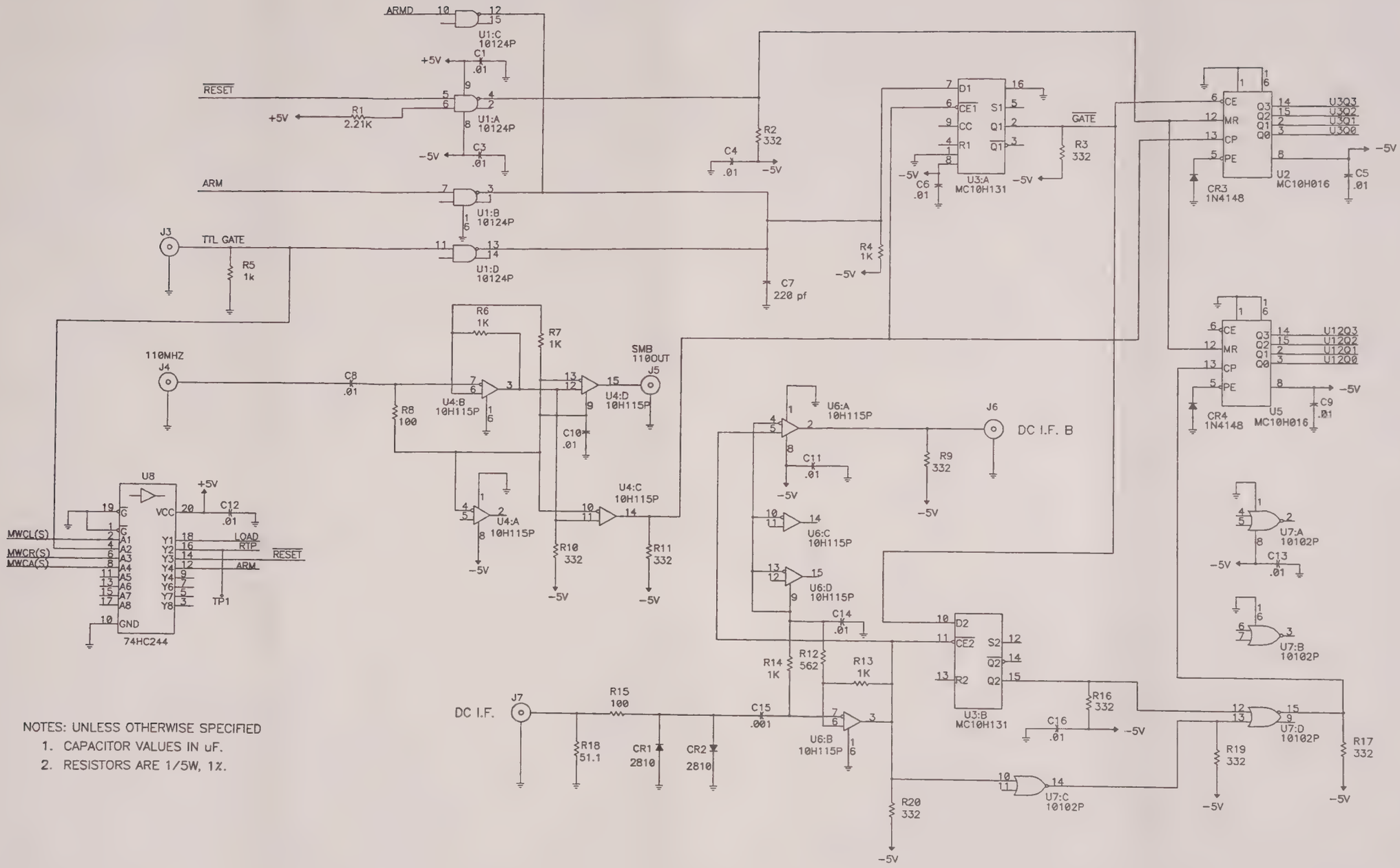
The buffered 110 MHz input (U4-14) is used to clock U2, a four-bit counter. This is the reference counter. The buffered I.F. input, as it propagates through U3-B and U7-D, is used to clock U5, the I.F. counter.

On sheet 4, the four output lines of the 110 MHz reference counter, received through RM1, are translated by U9 from ECL to TTL levels, and applied to U11, an integrated counter. U11 contains a cascade of counters and latches which enable it to count very large numbers, up to 32 bits long.

The four output lines of the I.F. counter, received through RM2, are translated from ECL to TTL by U14, and applied to U15, a counter identical to U11. However, the most significant bit line of the I.F. counter is divided by two (see U13A) in order to increase the range of the counter (the computer compensates for this division when it calculates the frequency of the I.F. input).

The outputs of the counter chips (U11 and U15) are furnished to the computer through buffer U10.

Addressing of the two counter chips is accomplished with the aid of the PROM (U18) shown on sheet 5. Several control lines from the computer are buffered by U17 and U20 and applied to the PROM, which translates them into select lines for the counter chips.

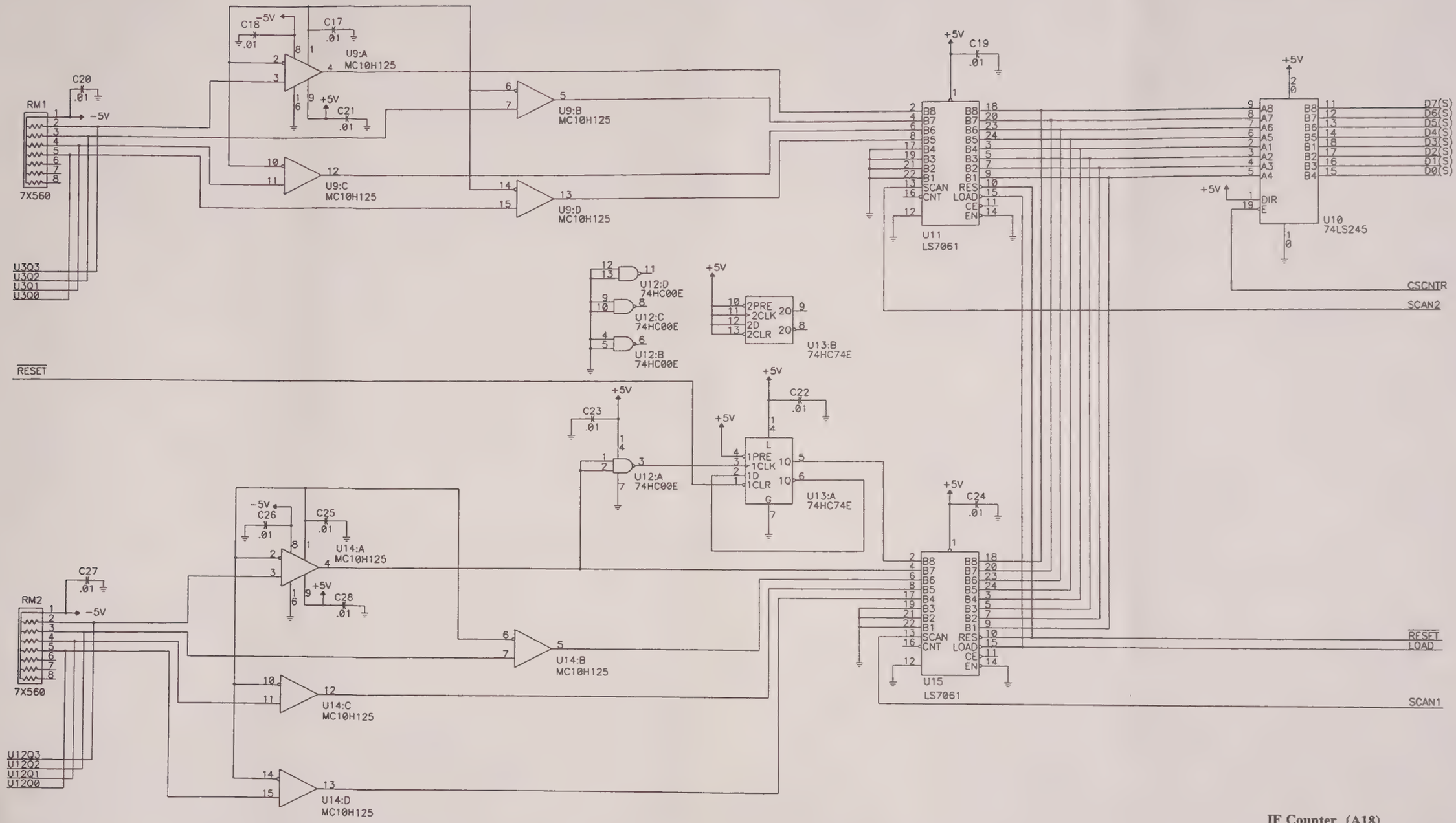


NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES IN uF.
2. RESISTORS ARE 1/5W, 1%.

IF Counter (A18)

DWG# 310BM11001 Rev 1

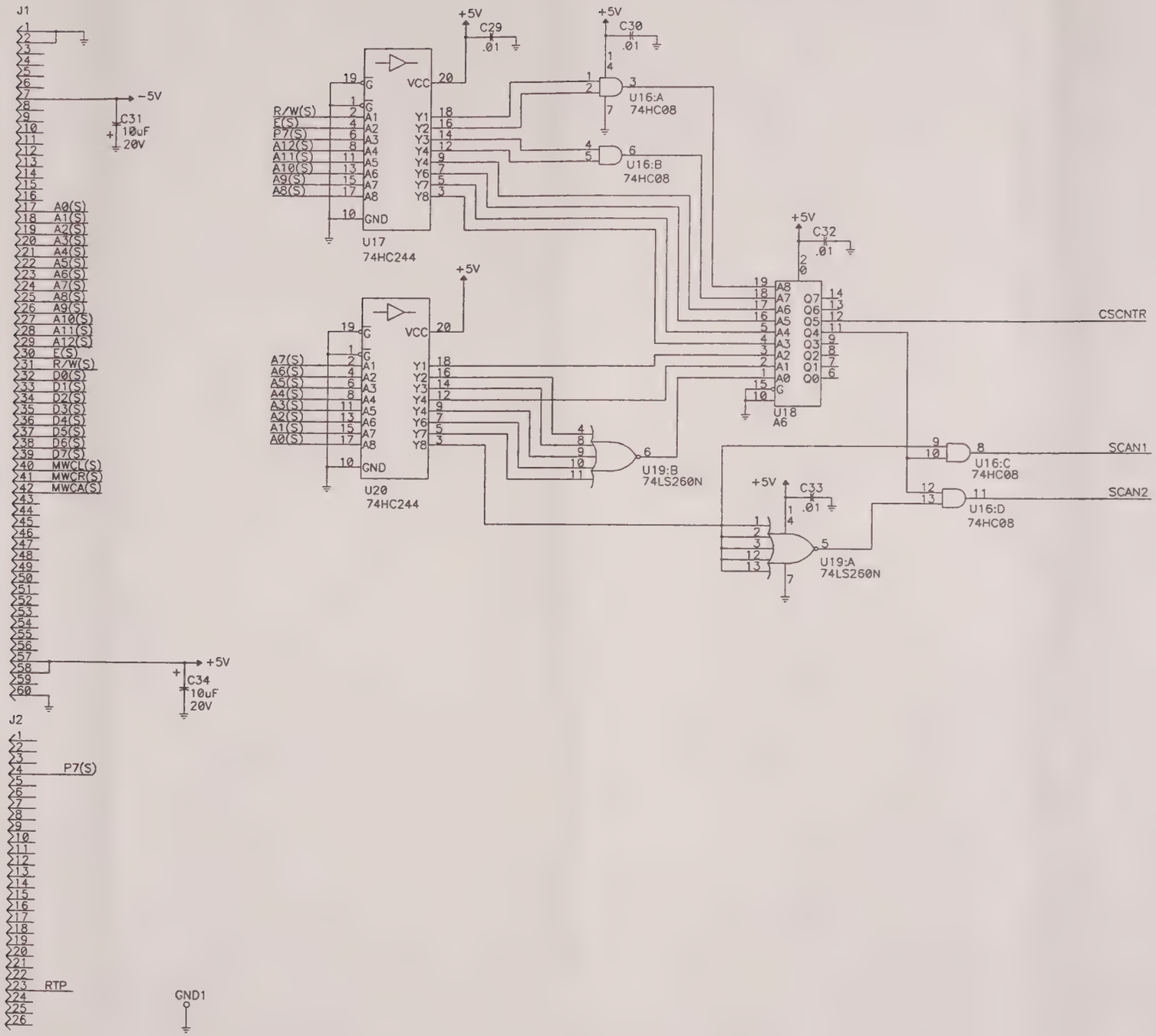


IF Counter (A18)

DWG# 310BM11001 Rev 1

Sheet 4 of 5

7-A18-4

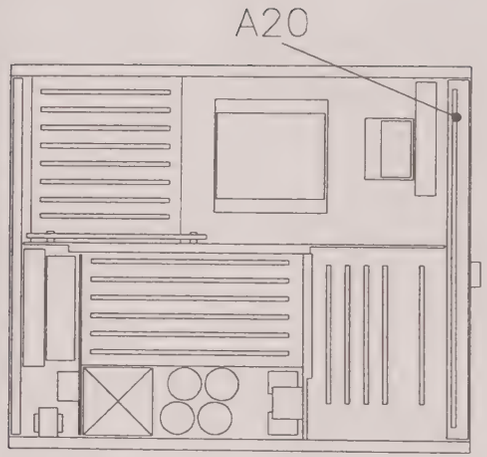


IF Counter (A18)

DWG# 310BM11001 Rev 1

Sheet 5 of 5

7-A18-5

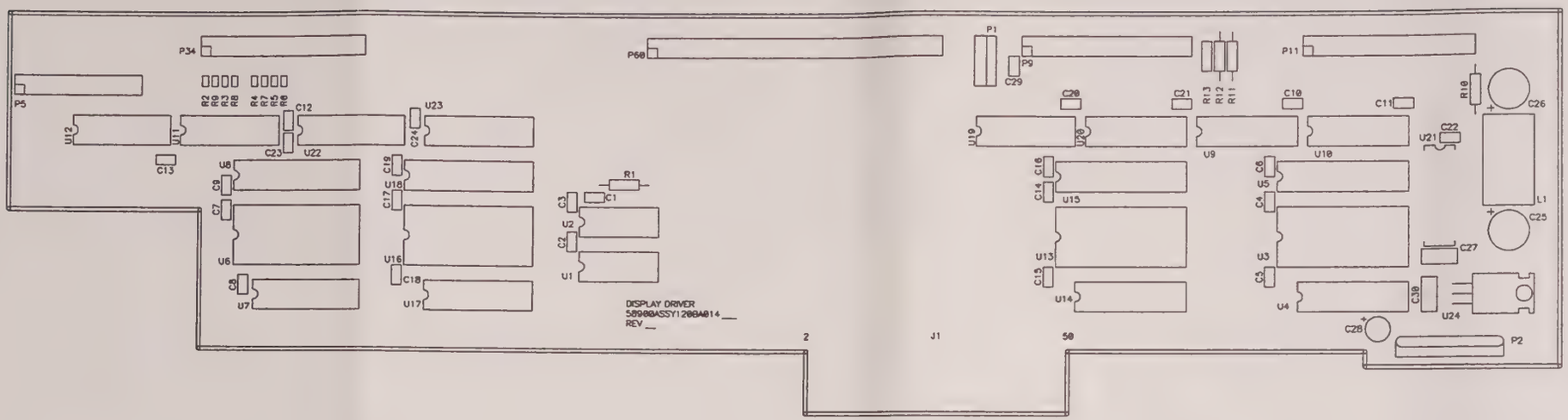


Display Driver (A20)

DWG# 120BM01401 Rev D

Sheet 1 of 4

7-A20-1

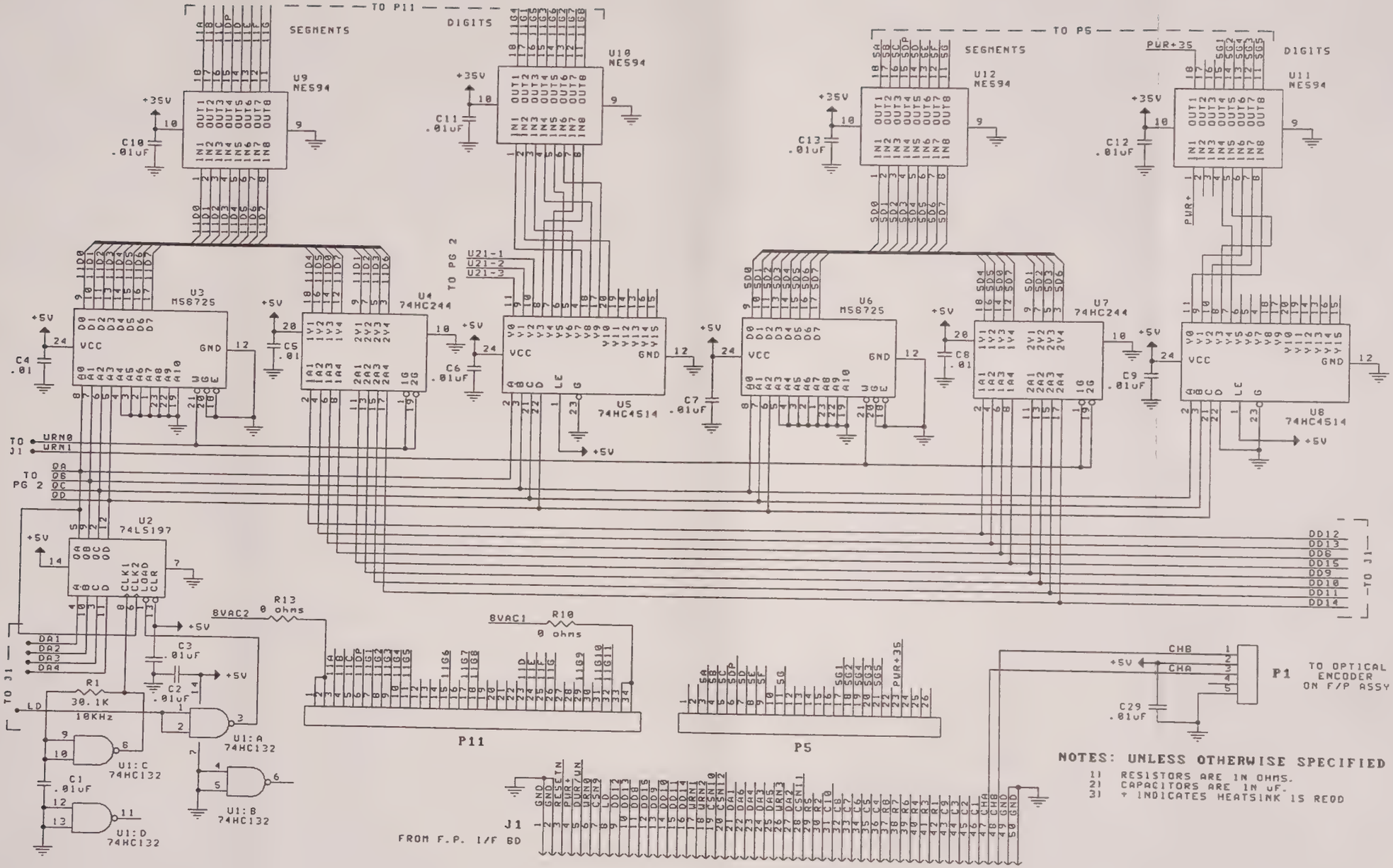


DISPLAY DRIVER -- PC ASSY A20

This board holds the necessary circuitry to drive the fluorescent displays and the LED's on the front panel.

U2 is a counter which is clocked by U1 thereby cycling thru the addresses corresponding to each display digit and its segments. When the computer updates the display or when a setting has been changed, the LD line is activated, and the counter U2 stops counting and outputs the address which is on its A-D inputs, to QA-QD outputs thus addressing the decoders and RAMS when the appropriate chips are selected by the read/write lines. At this time data is available at the input of the latch U4 and can be loaded into the RAM U3. When the data has been updated for all addresses, the LD line becomes inactive and the counter U2 again cycles thru the addresses, selecting data for specific segments to be driven via U9. At the same time decoder U5 decodes the addresses to select each individual digit via U10. This scheme is used to drive all 3 fluorescent displays.

A similar scheme is used for lighting the LED's on the front panel; the only difference is that they are addressed by rows and columns via U22 and U23 respectively.



NOTES: UNLESS OTHERWISE SPECIFIED

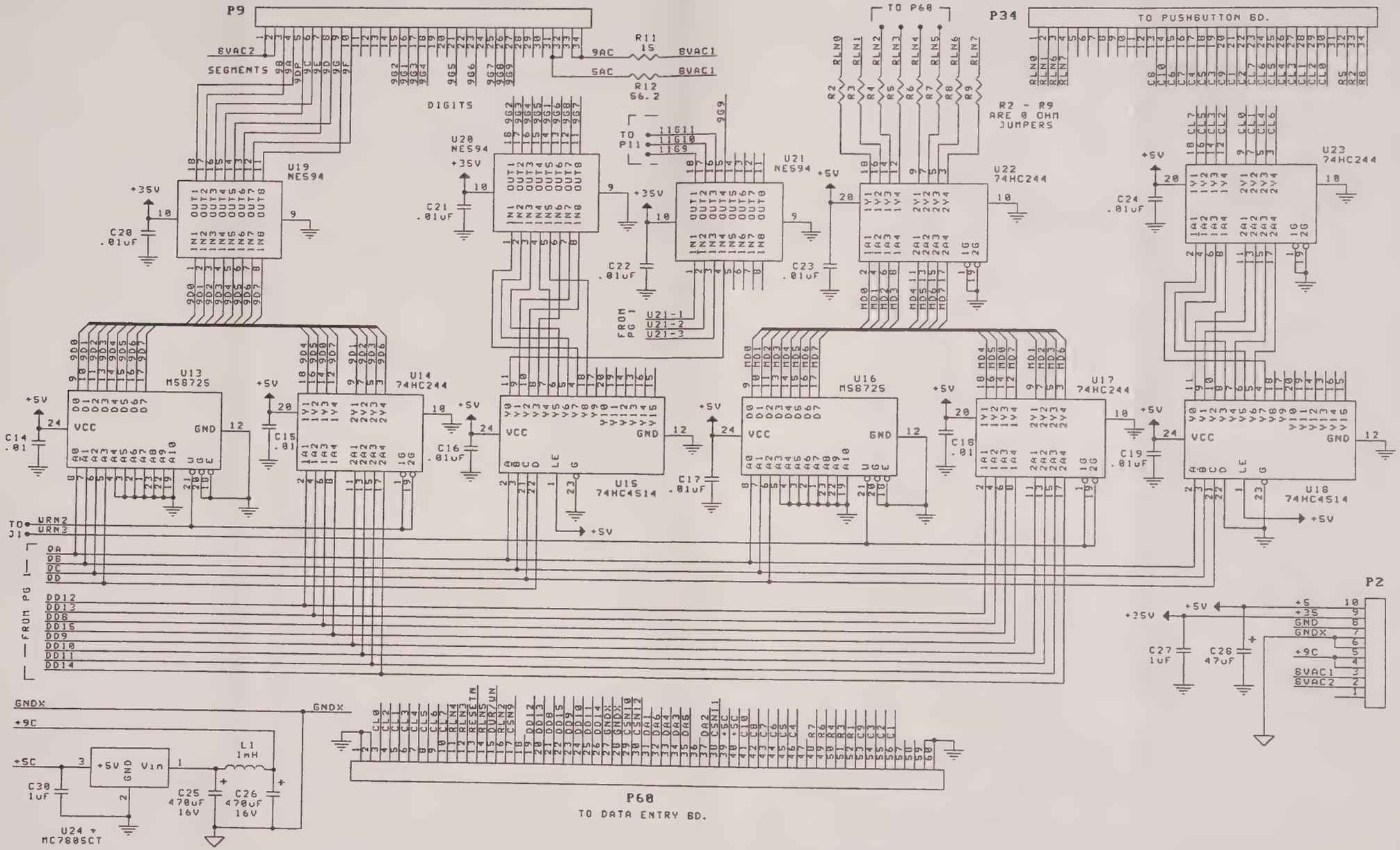
1) RESISTORS ARE IN OHMS.
2) CAPACITORS ARE IN uF.
3) * INDICATES HEATSINK IS REQD

Display Driver (A20)

DWG# 120BM01401 Rev D

Sheet 3 of 4

7-A20-3

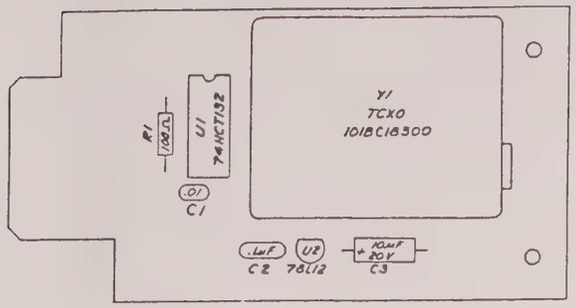


Display Driver (A20)

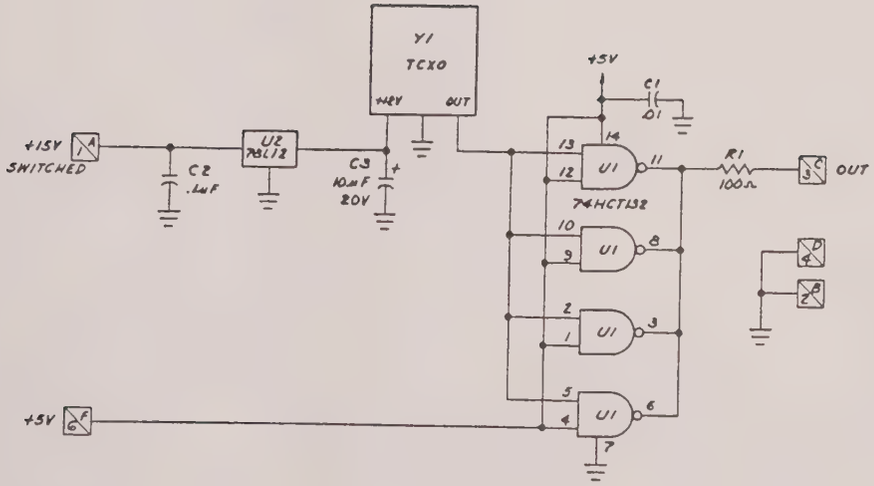
DWG# 120BM01401 Rev D

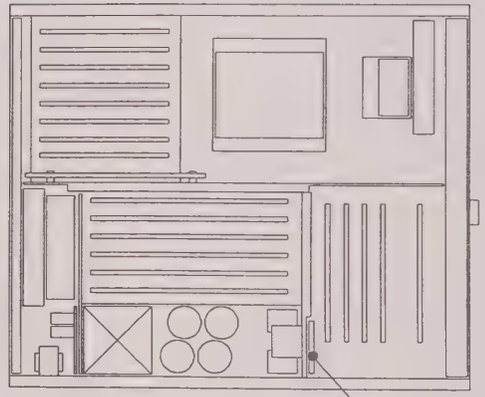
Sheet 4 of 4

7-A20-4



NOTES: UNLESS OTHERWISE SPECIFIED
1.) CAPACITOR VALUES IN uF
2.) RESISTOR VALUES IN OHMS



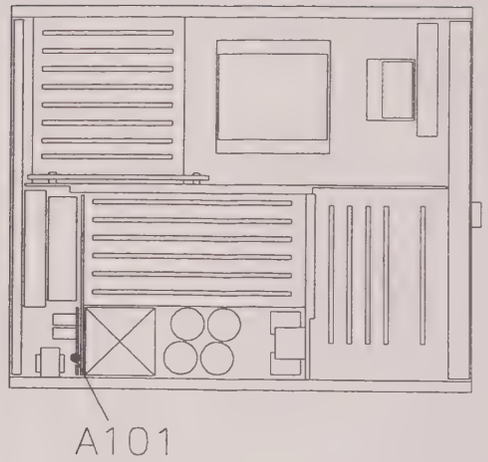


TCXO (A32)

DWG# 101BM09702 Rev B

Sheet 1 of 1

7-A32-1

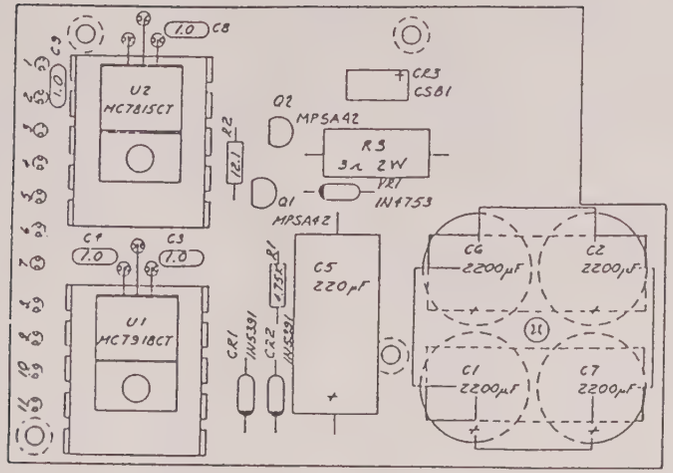


Power Supply (A101)

DWG# 304BM01100 Rev E

Sheet 1 of 2

7-A101-1



NOTE: The schematic diagram for this circuit is incorporated in the Power Supply Assy diagram (DWG# 310BM14100, p. 7-11).

POWER SUPPLY -- PC ASSY A101

Many of the components which make up the power supply are not located on the power supply circuit board because of their large size or cooling requirements. The line filter is attached to the rear panel. The transformer and the filter capacitors are mounted along the left side of the instrument, near the computer circuits. The rectifiers and voltage regulators are mounted on the heat sink at the rear of the instrument.

The transformer secondary voltages are rectified, filtered and applied to voltage regulators to produce the instrument's power supply outputs:

Q5 provides the +5V supply used by the RF circuits.

Q1 provides the +5V supply used by the computer.

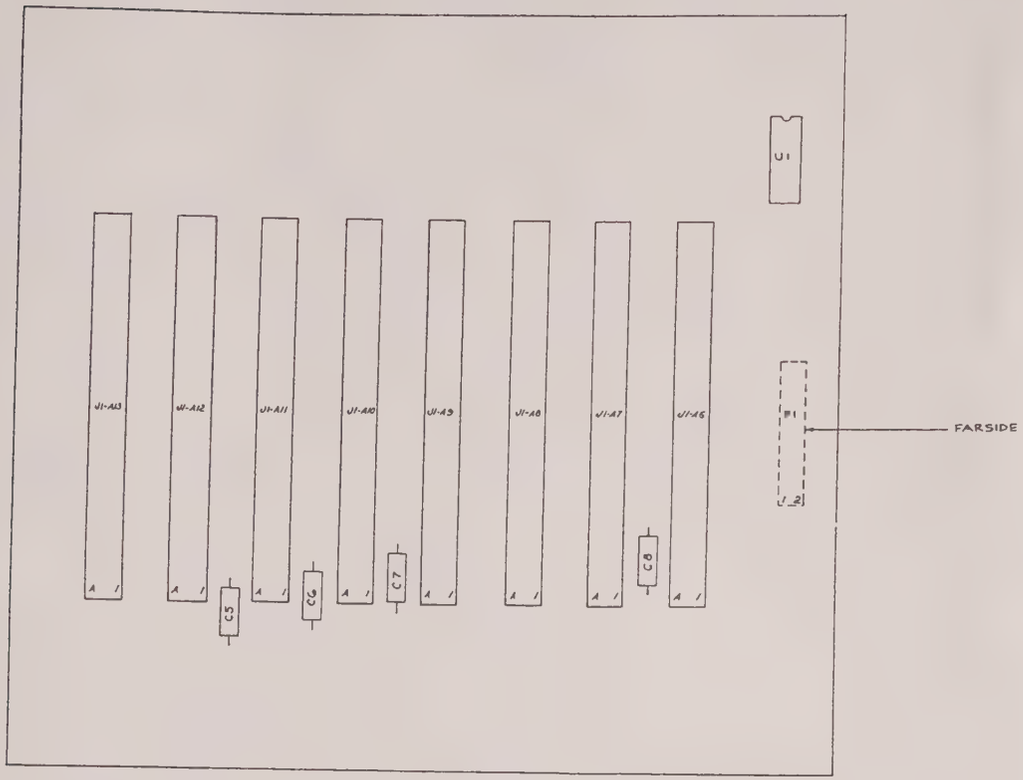
Q2 provides the -5.2V supply used by the RF circuits.

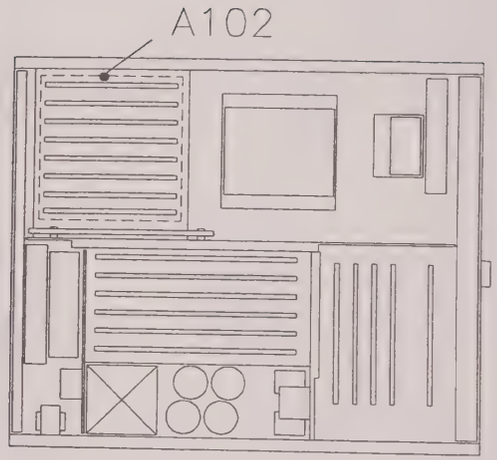
Q3 provides the +18V supply used by the RF circuits.

Q4 provides the +18V supply used by the VCO's.

U1 provides the -18V supply used by the RF circuits.

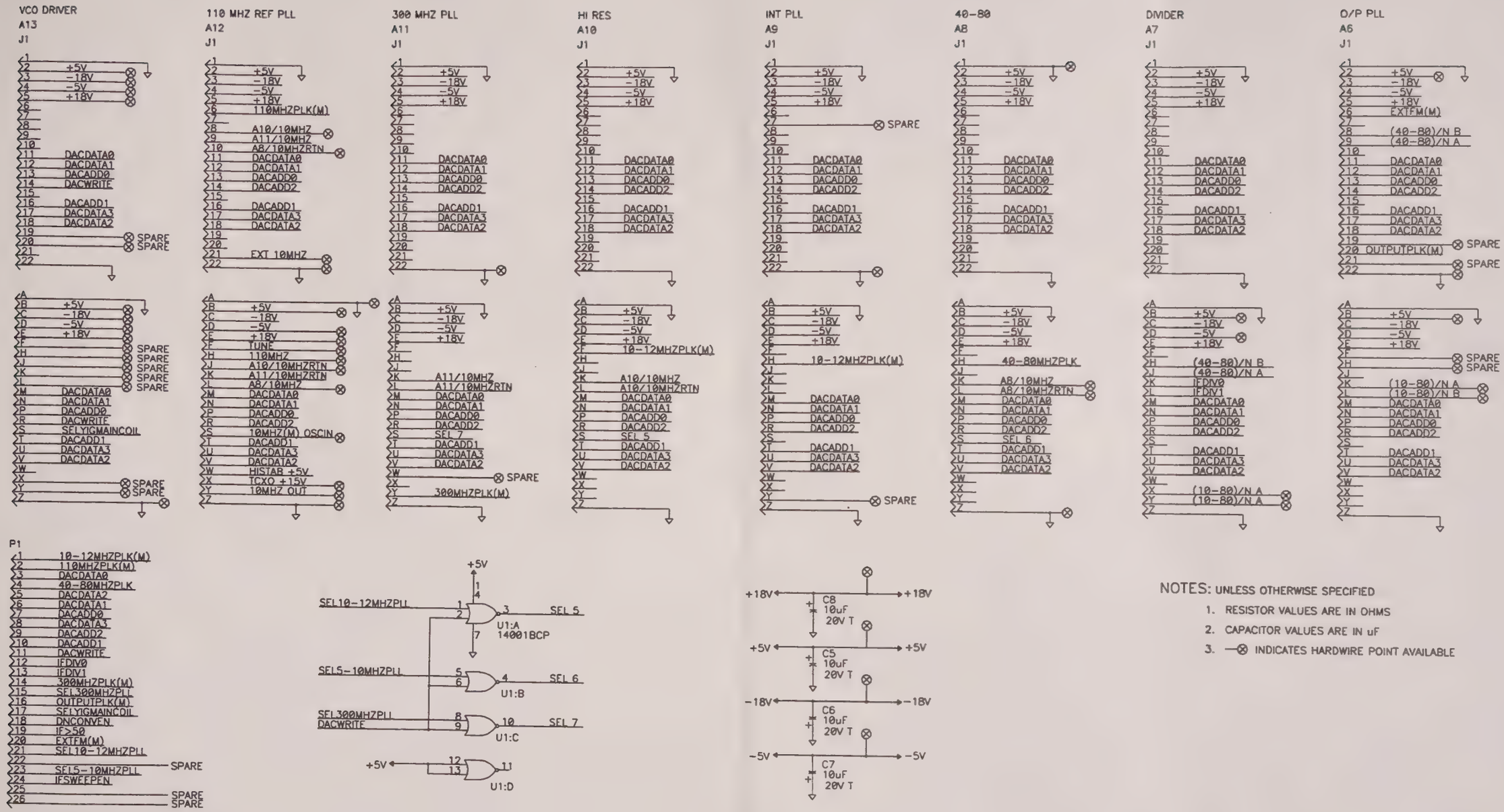
REGULATED SUPPLIES: The +35V and 8VAC supplies are used by the fluorescent displays on the front panel. The +24V supply is used by the cooling fan and by the relays in the 10 dB step attenuator.





RF Bus (A102)

DWG# 304BM02902 Rev B



NOTES: UNLESS OTHERWISE SPECIFIED

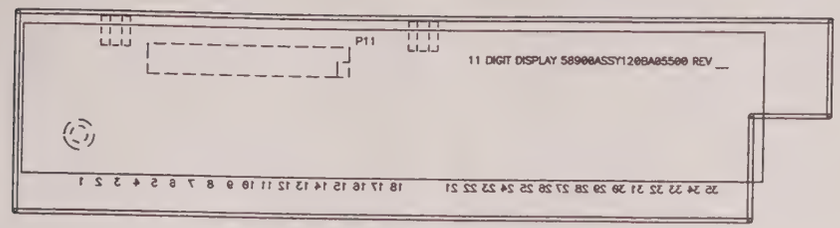
1. RESISTOR VALUES ARE IN OHMS
2. CAPACITOR VALUES ARE IN uF
3. —⊗ INDICATES HARDWIRE POINT AVAILABLE

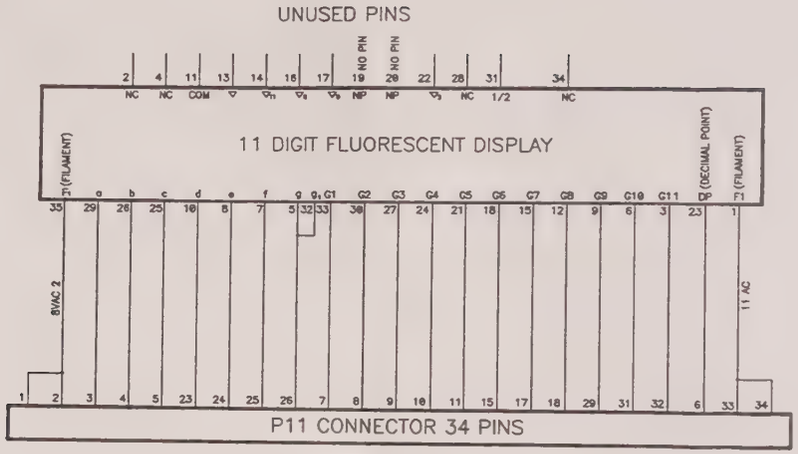
RF Bus (A102)

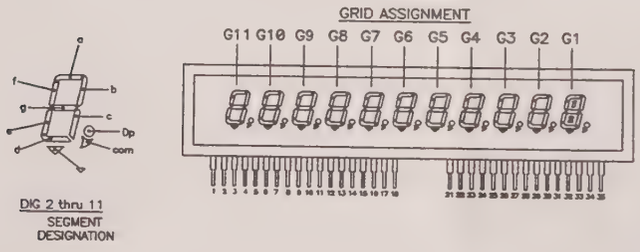
DWG# 304BM02902 Rev B

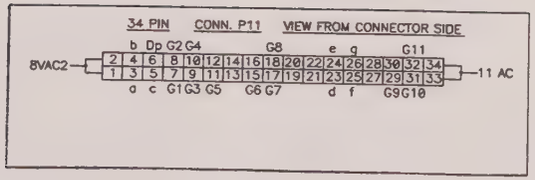
Sheet 2 of 2

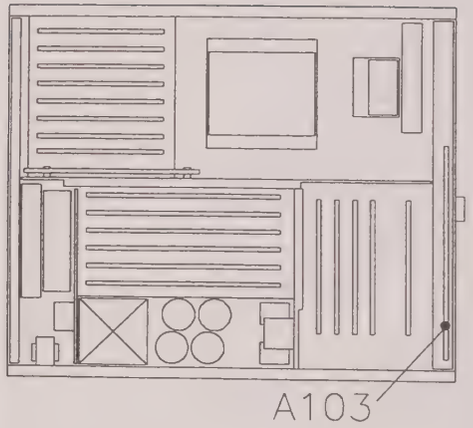
7-A102-2









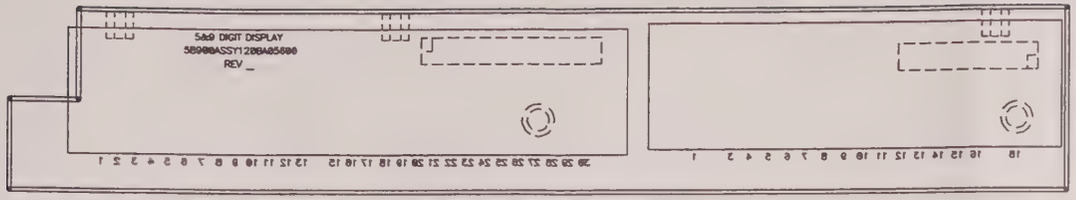


11 Digit Display (A103)

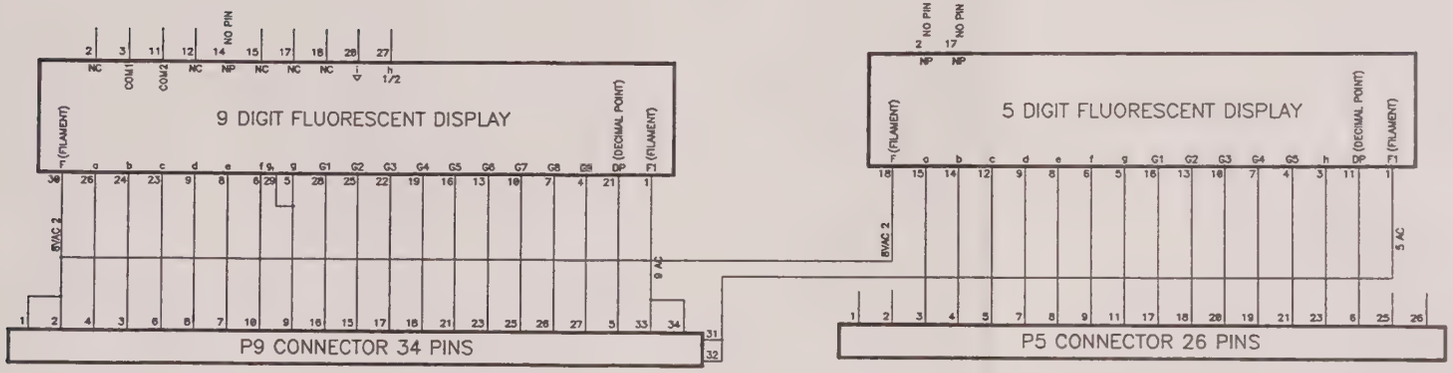
DWG# 120BM05500 Rev C

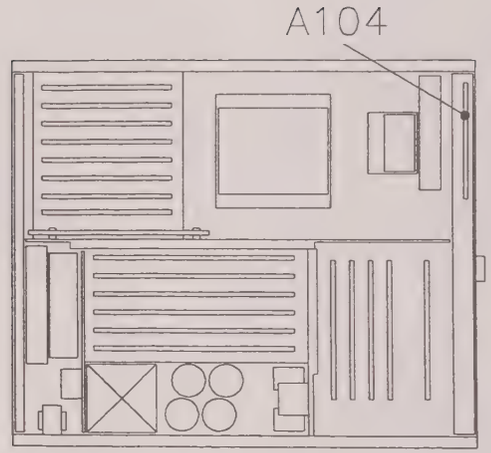
Sheet 1 of 1

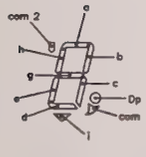
7-A103-1

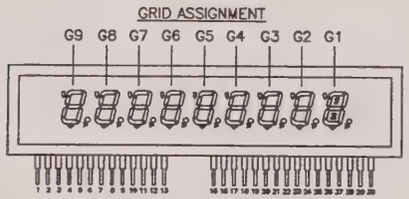


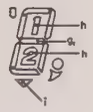
UNUSED PINS

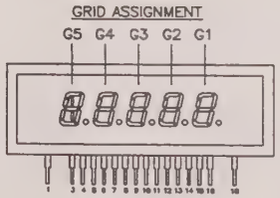


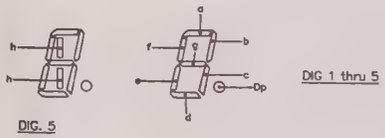


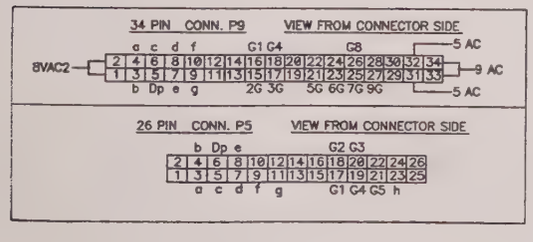










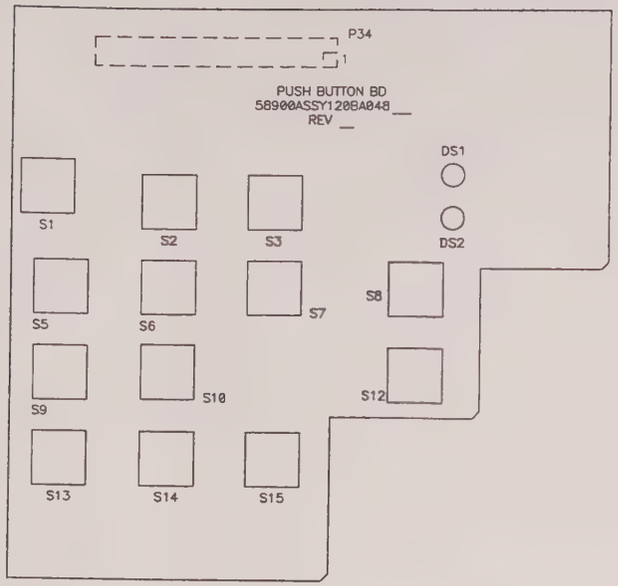


5 & 9 Digit Display (A104)

DWG# 120BM05600 Rev C

Sheet 1 of 1

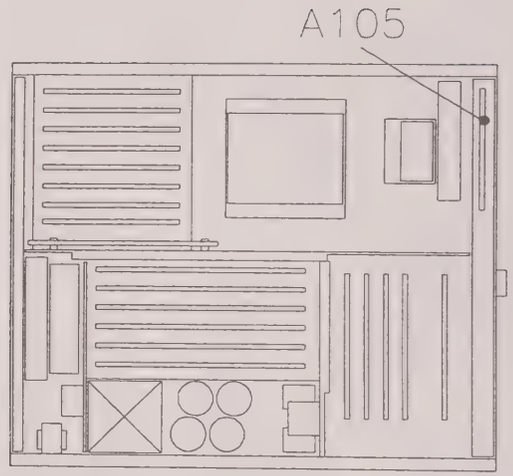
7-A104-1

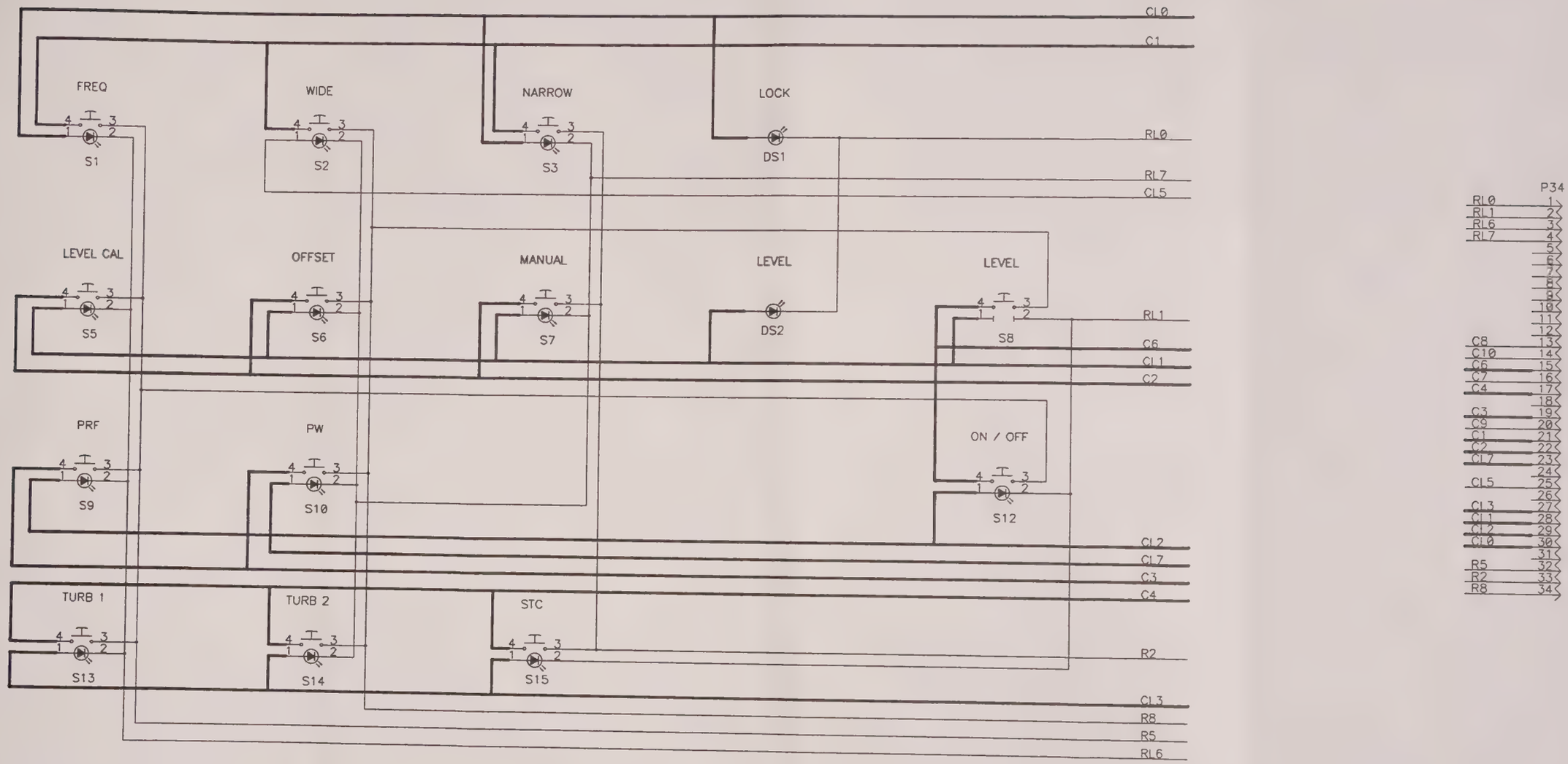


PUSH BUTTON -- PC ASSY A105

The Push Button board holds the push buttons for the level buttons and their corresponding LED's as well as the LOCK and LEVEL LED's.

The buttons are connected together such that they can be read and identified using a row and column scheme. The LED's are set up the same way using a row and column scheme (denoted RL and CL) to light the appropriate LED's.



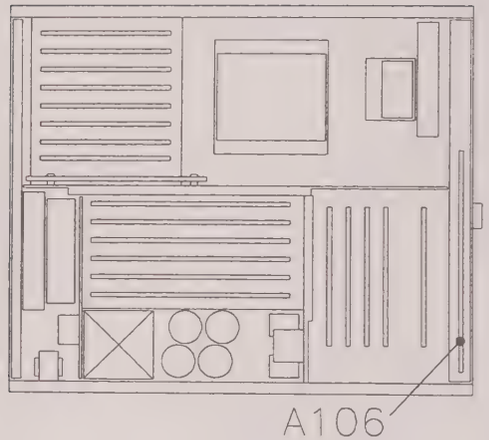


Push Button (A105)

DWG# 120BM04805 Rev B

Sheet 2 of 2

7-A105-2

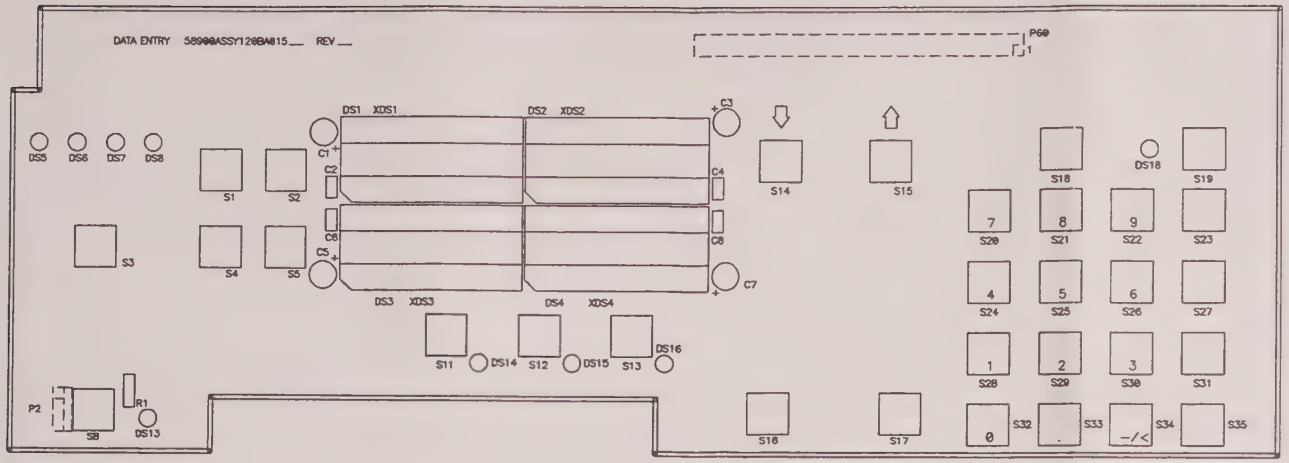


Data Entry (A106)

DWG# 120BM01514 Rev B

Sheet 1 of 4

7-A106-1

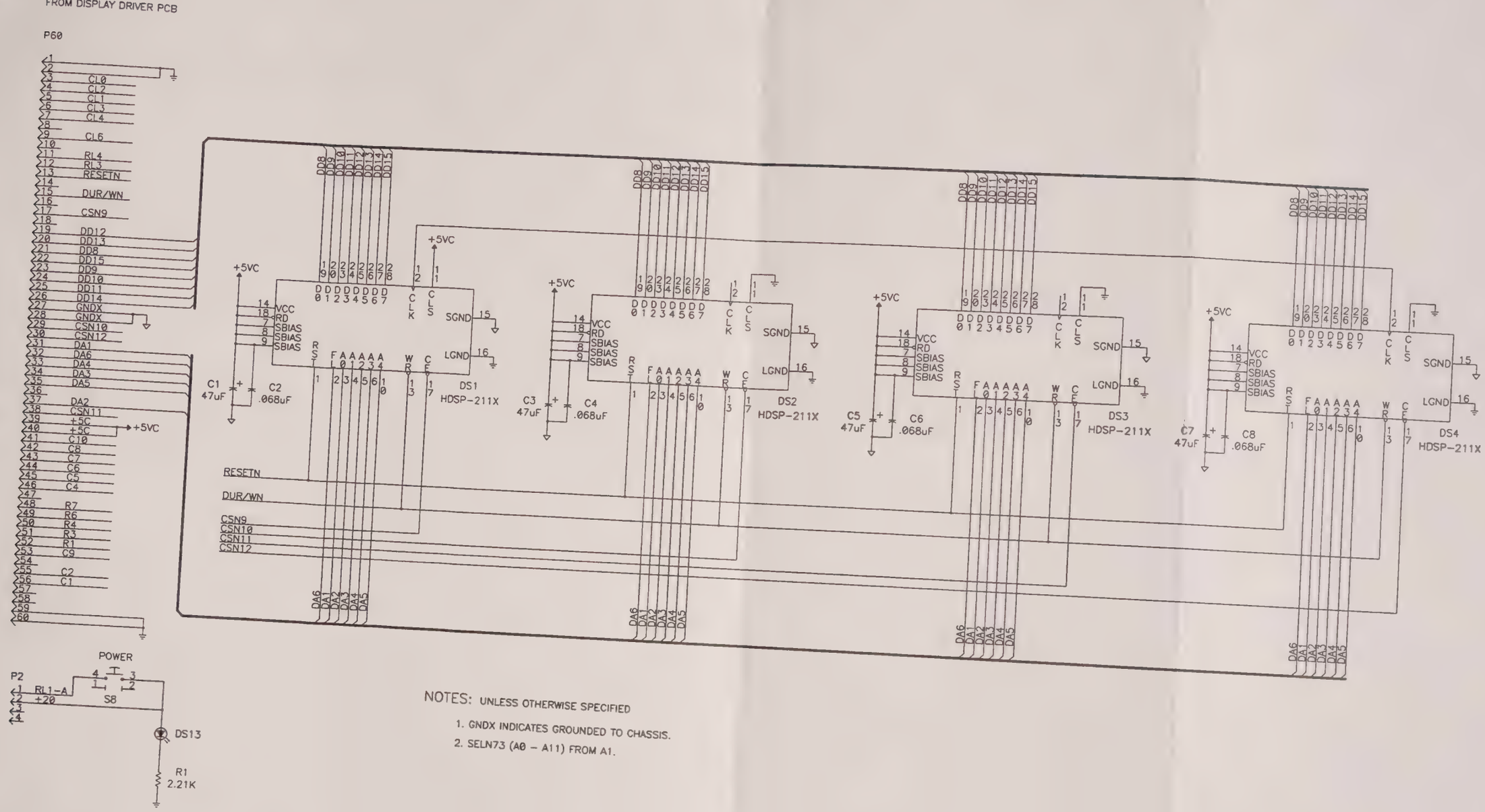


DATA ENTRY -- PC ASSY A106

This board holds the push buttons for the keypad as well as any corresponding LEDs. In addition the Intelligent HP alpha numeric displays reside on this board.

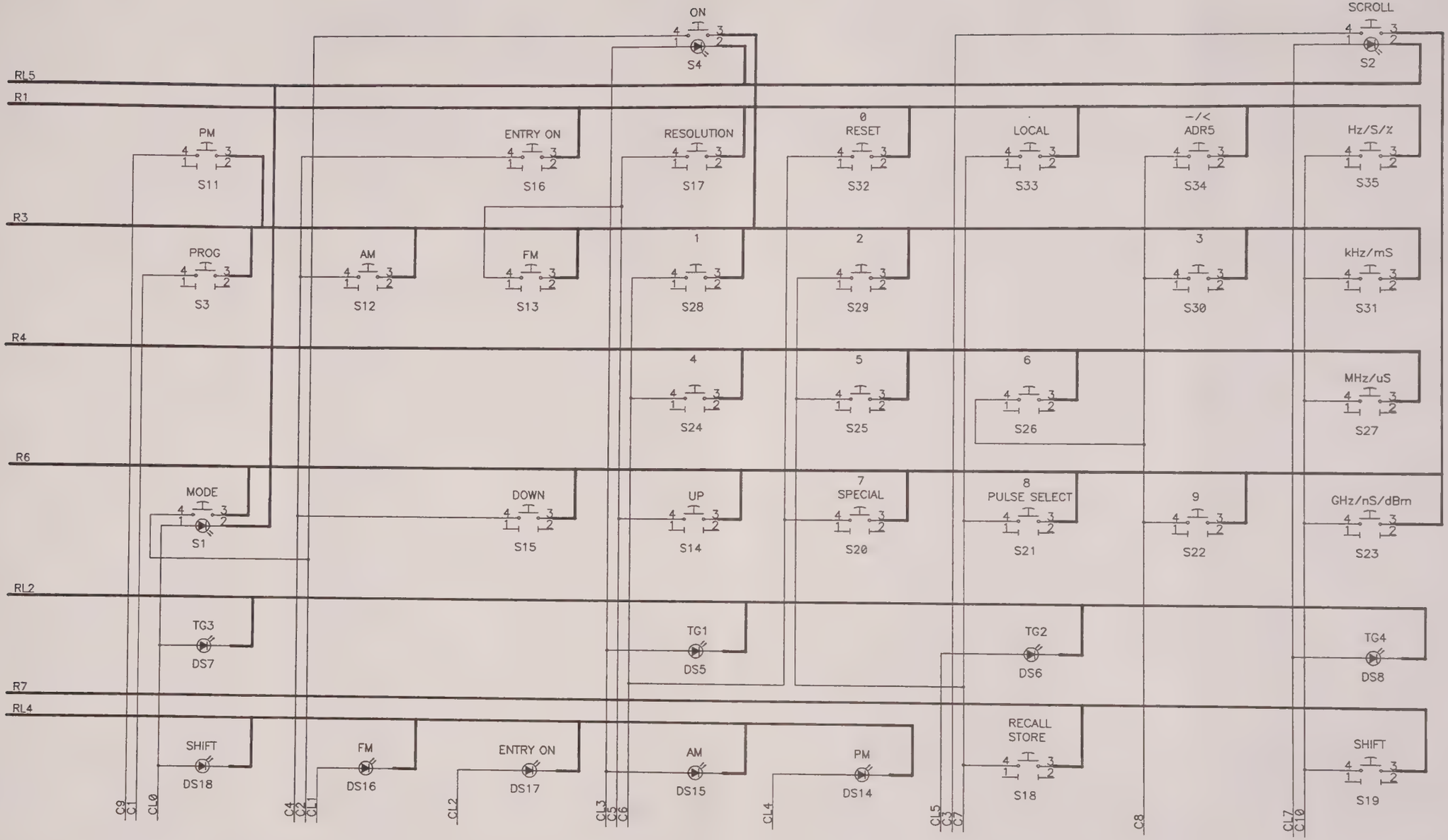
As on the Push Button Board A105, the push buttons are read and the LEDs are lit using the rows and columns scheme. The two 8 digit Intelligent HP alpha numeric displays (DS1-DS4) receive address and data information from the Keyboard/LED VIA board.

When the unit has power applied to it the standby LED DS13 is lit by an unregulated positive voltage from the power supply via P2. When the Power switch is activated the voltage coming in on P2 is switched to energize the power relay switch which supplies power to the rest of the Unit.



NOTES: UNLESS OTHERWISE SPECIFIED

1. GNDX INDICATES GROUNDED TO CHASSIS.
2. SELN73 (A0 – A11) FROM A1.

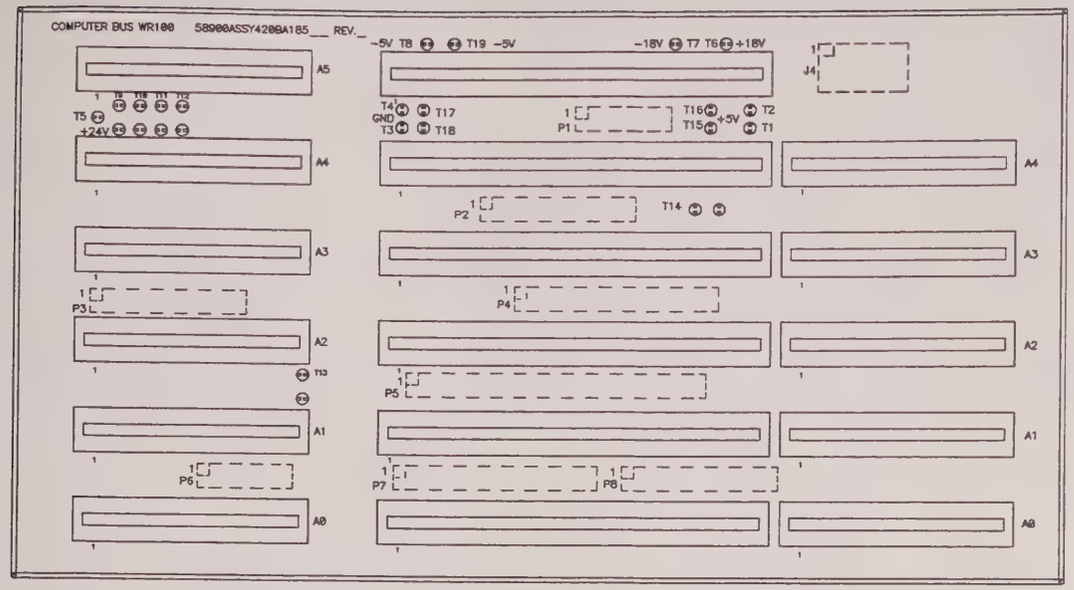


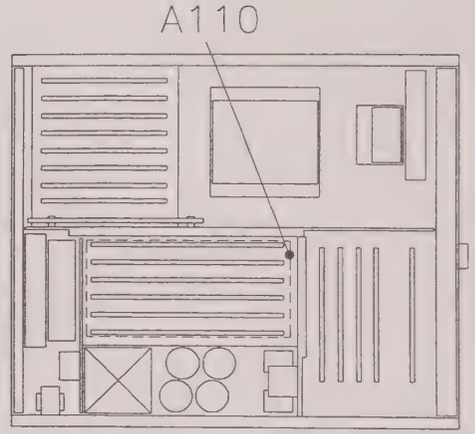
Data Entry (A106)

DWG# 120BM01514 Rev B

Sheet 4 of 4

7-A106-4





Computer Bus (A110)

DWG# 420BM18500 Rev A

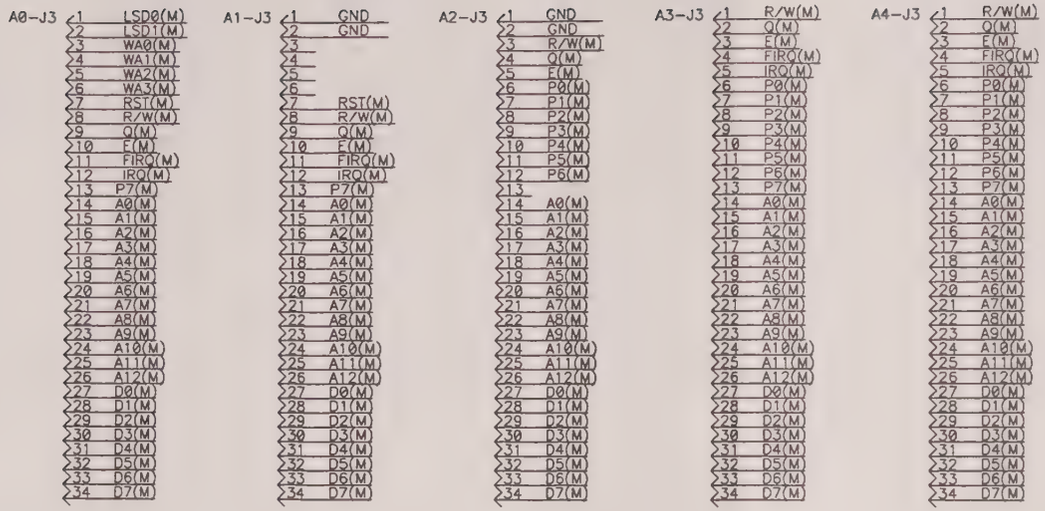
Sheet 1 of 3

Computer Bus (A110)

DWG# 420BM18500 Rev A

Sheet 2 of 3

7-A110-2



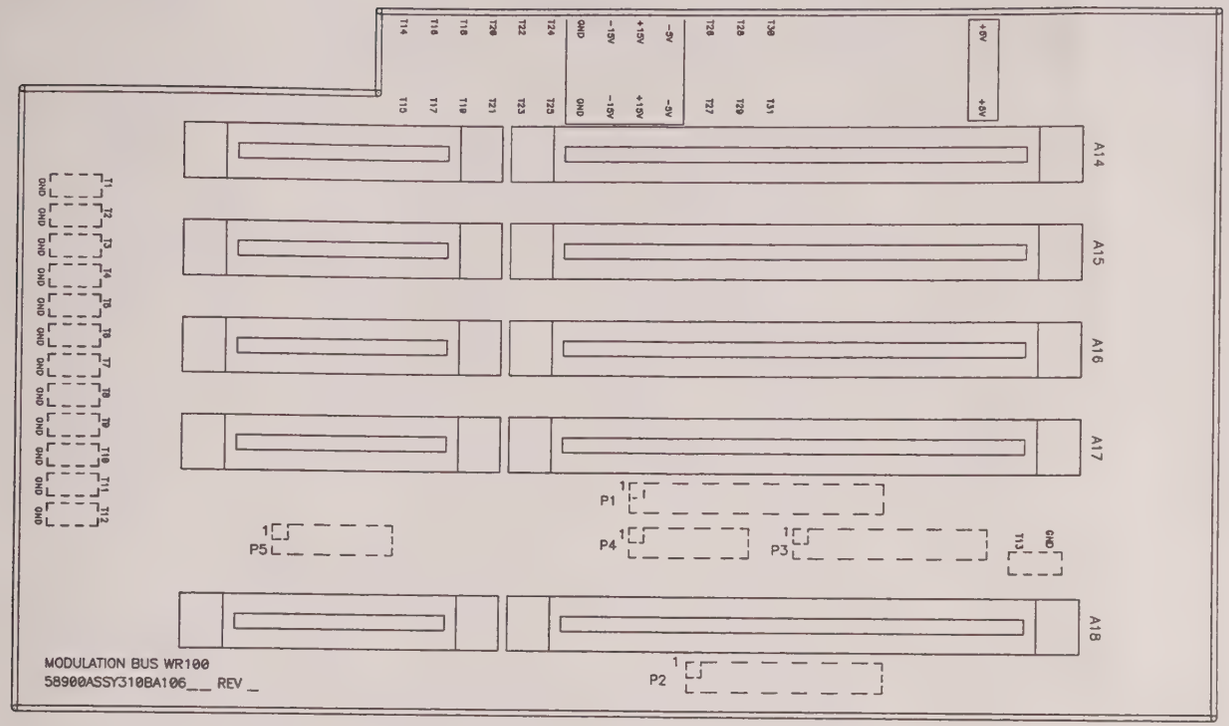
DUAL MICROPR0C (128K)	A4
IEEE PIA	A3
MEMORY	A2
KEYBD/VIA	A1
VIA	A0

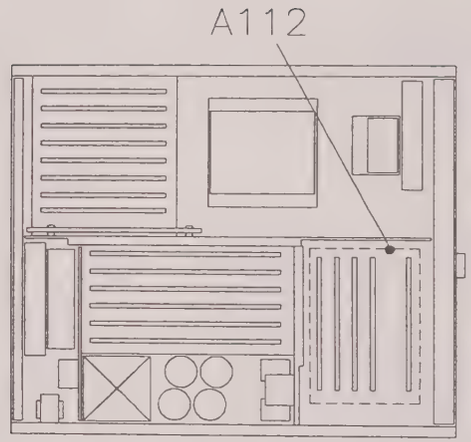
Computer Bus (A110)

DWG# 420BM18500 Rev A

Sheet 3 of 3

7-A110-3



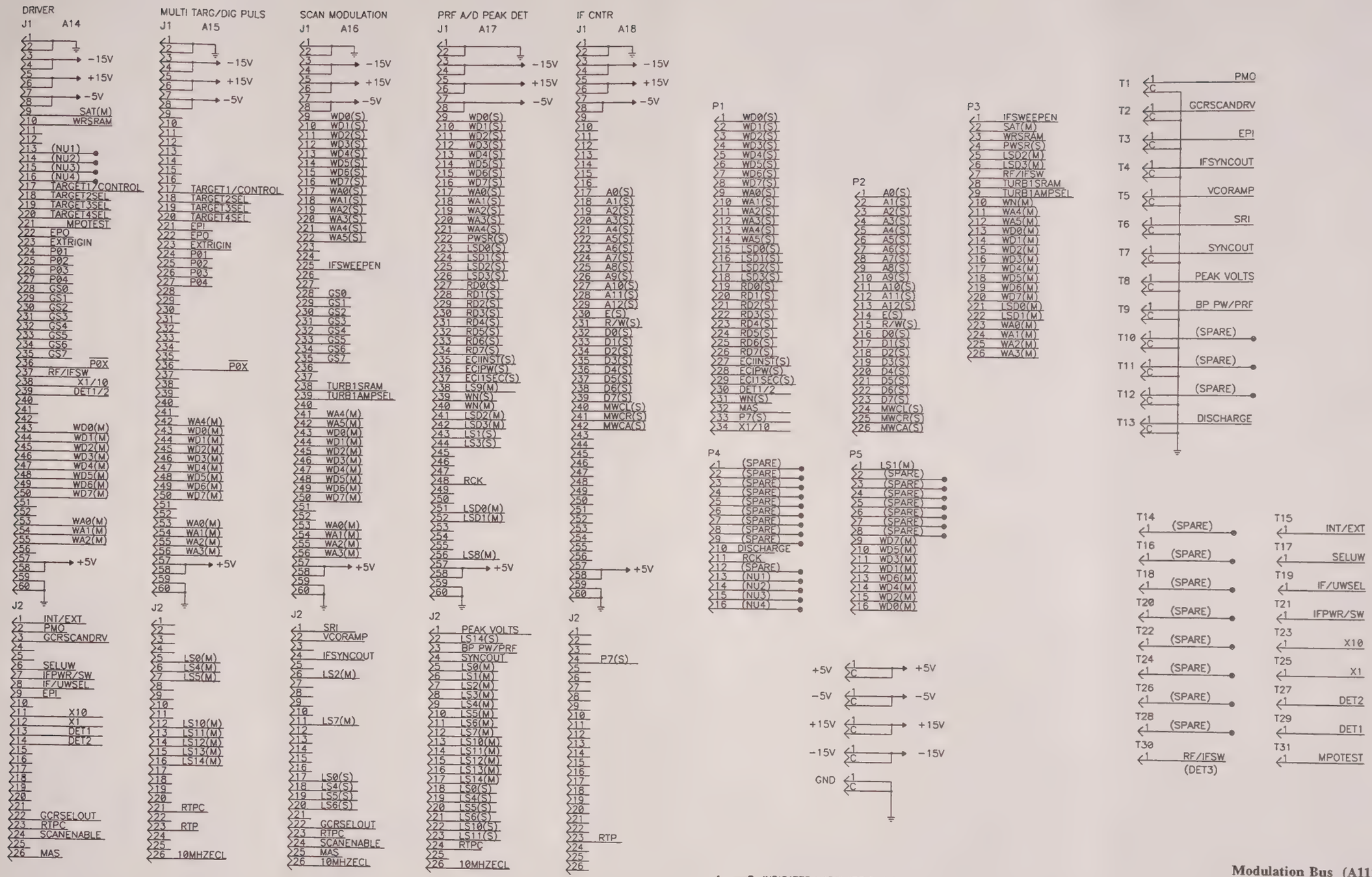


Modulation Bus (A112)

DWG# 310BM10600 Rev A

Sheet 1 of 2

7-A112-1



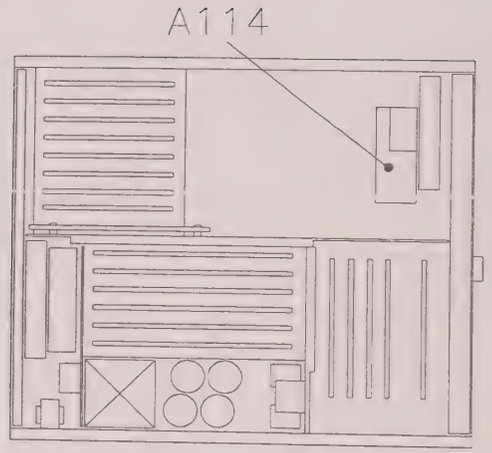
1. ● INDICATES HARDWIRE PAD AVAILABLE ON PCB

Modulation Bus (A112)

DWG# 310BM10600 Rev A

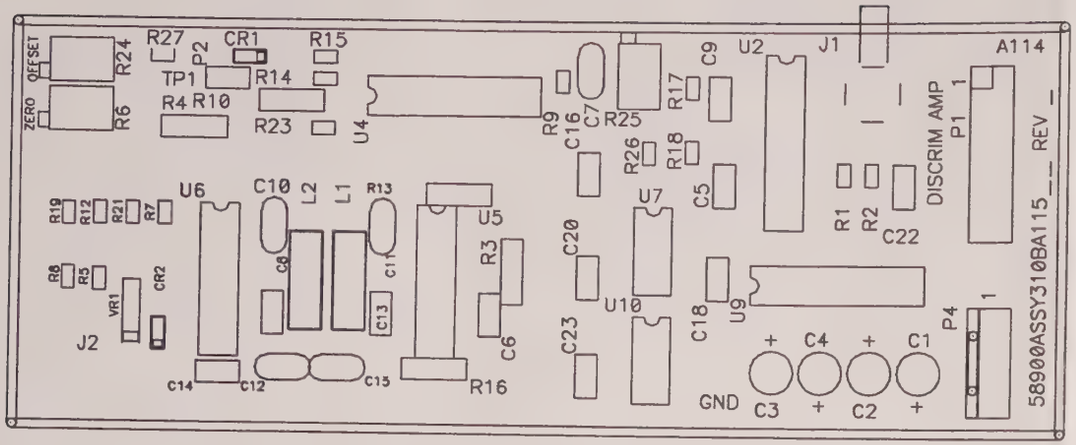
Sheet 2 of 2

7-A112-2



Discriminator Amp (A114)

DWG# 310BM11510 Rev A

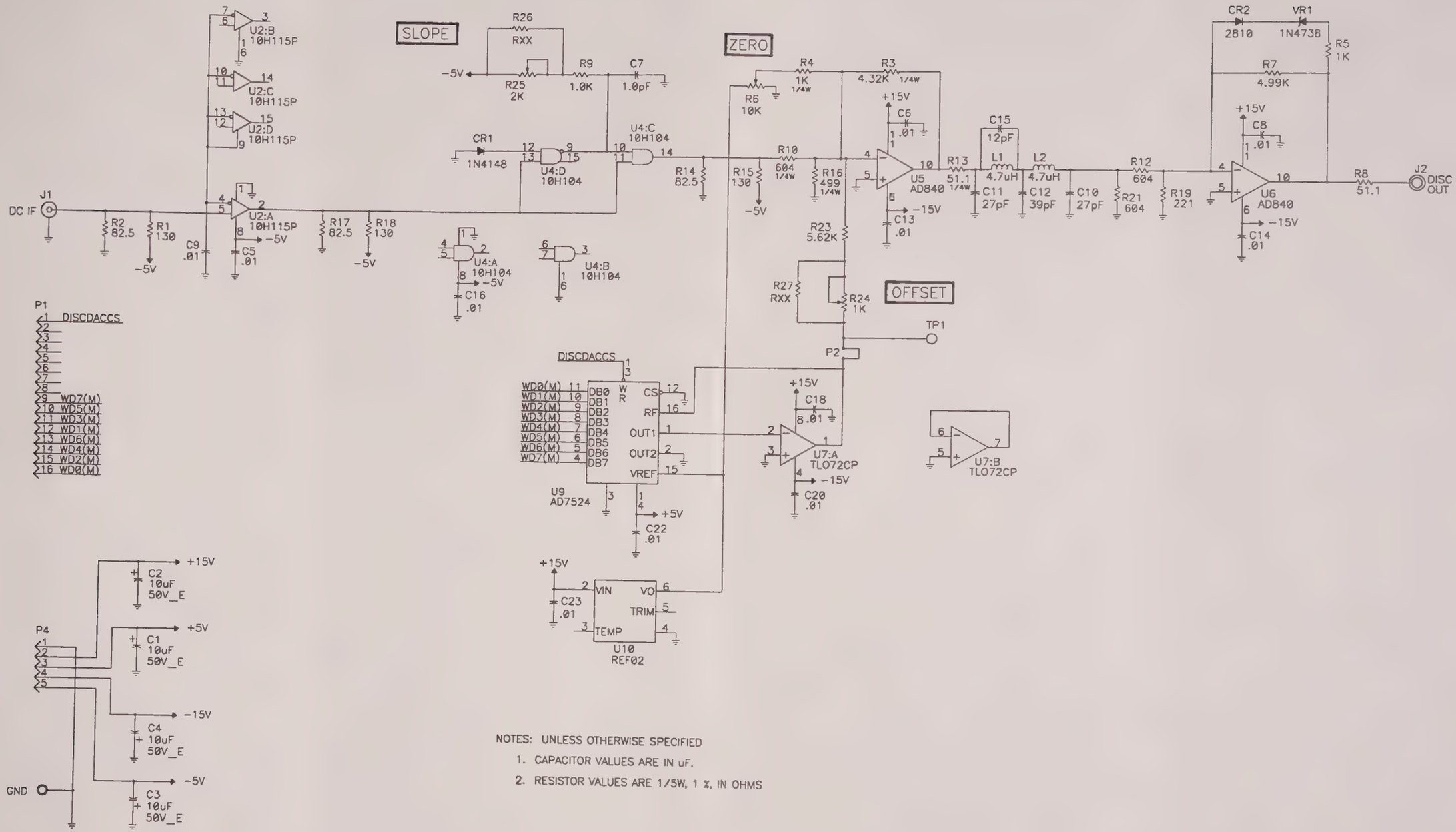


DISCRIMINATOR AMPLIFIER -- PC Assembly A114

This circuit produces a voltage output which is derived from the frequency counter IF. The voltage output can be used to monitor changes in the incoming radar frequency.

The downconverter IF from the frequency is received at J1 and buffered by U2A. The pulse-narrowing circuit consisting of U4C and U4D produces narrow pulses triggered by the edges of the IF signal; this results in pulses of uniform width and amplitude, but with frequency determined by the IF frequency. These pulses are amplified by U5 and converted into a DC voltage by a low pass filter (see L1, L2, etc.). The voltage produced by the filter is proportional to the frequency of the input pulses. This voltage is provided, via amplifier U6, to the discrimminator output (J2).

The amplifier consisting of U5 includes a programmable offset input; the offset is determined by the CPU when it programs DAC U9. The offset is used by the CPU to position the desired frequency at a level of zero volts on the discriminator output. In this way, the discriminator can display drift away from the set radar frequency as drift away from zero volts.



NOTES: UNLESS OTHERWISE SPECIFIED

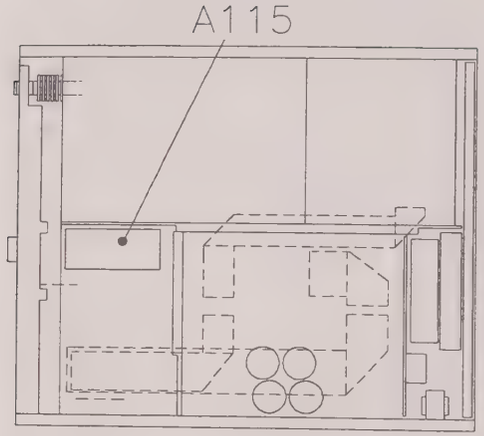
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE 1/5W, 1 %, IN OHMS

Discriminator Amp (A114)

DWG# 310BM11510 Rev A

Sheet 3 of 3

7-A114-3

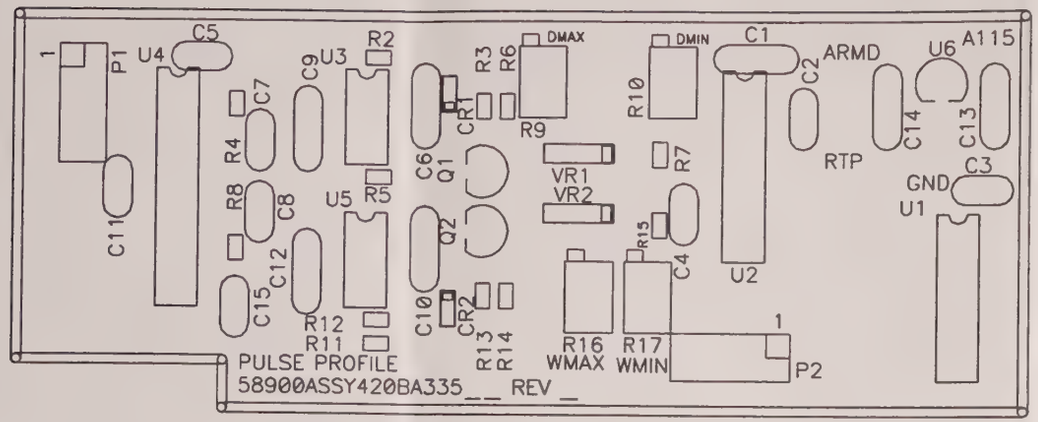


Pulse Profile (A115)

DWG# 420BM33500 Rev 1

Sheet 1 of 3

7-A115-1

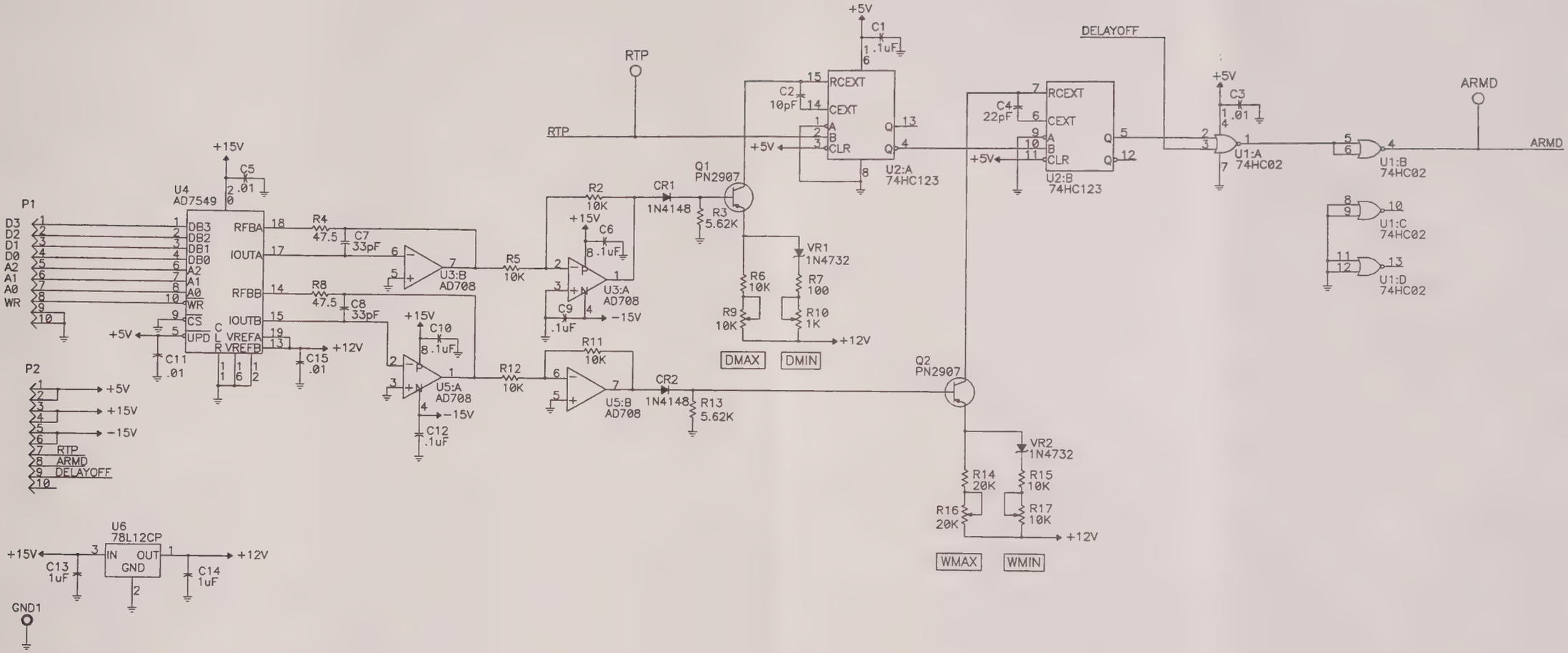


PULSE PROFILE -- PC Assembly A115

Magnetrons typically used in radar sets have a somewhat irregular frequency profile; the frequency of a radar pulse tends to be too high or low at the beginning and end of the pulse. In order to compensate for this irregularity, the Pulse Profile circuit generates a signal ('ARMD') which defines a count window for the frequency counter; this count window excludes approximately the first 10% and last 10% of the pulse from the count.

U4 is a dual DAC, which converts the binary numbers programmed by the CPU into two analog signals, amplified by U3 and U5. The amplifier outputs drive two current-source circuits (see Q1 and Q2). The current sources control a pair of one-shot IC's, U2A and U2B, triggered by the Radar Trigger Pulse. U2A provides a 'delay' interval, and U2B provides a 'width' interval. By programming the two halves of the DAC, the CPU sets the beginning and end of the count window with regard to the beginning and end of the RTP.

Delay and width are calibrated by means of 'max' and 'min' potentiometers in the current-source circuits.

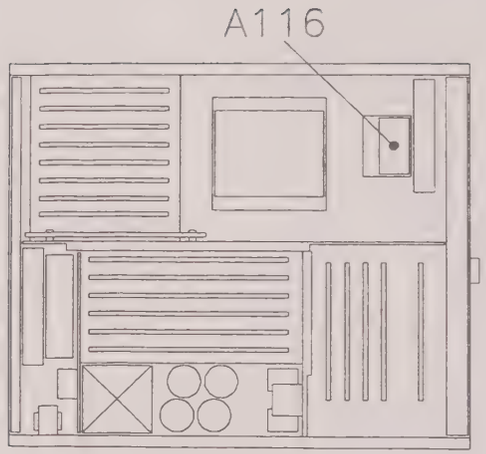


Pulse Profile (A115)

DWG# 420BM33500 Rev 1

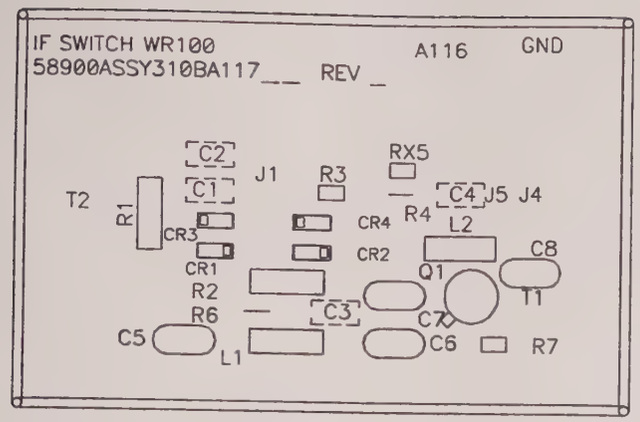
Sheet 3 of 3

7-A115-3



IF Switch (A116)

DWG# 310BM11710 Rev C

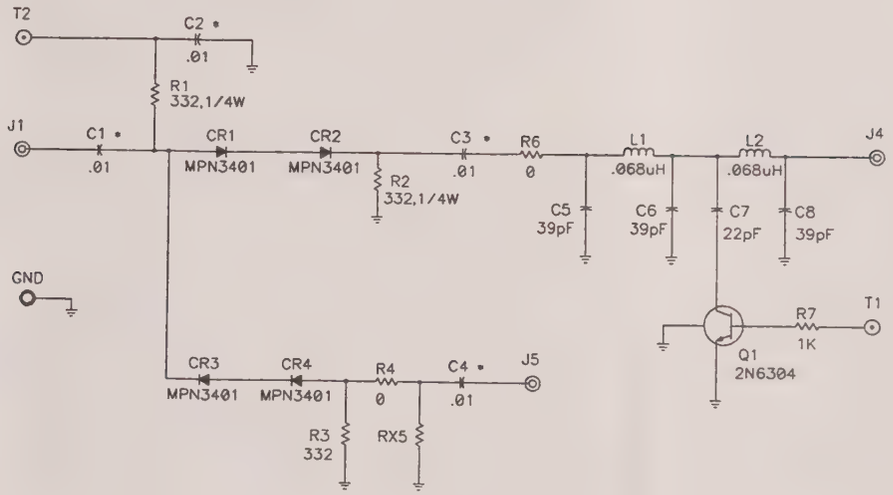


IF SWITCH -- PC ASSY A116

This circuit is used for path switching of the downconverter's IF output. The IF is received at J2. The two output paths lead to J5 (if the Generate mode is selected) or to J4 (if Track or Manual modes are selected).

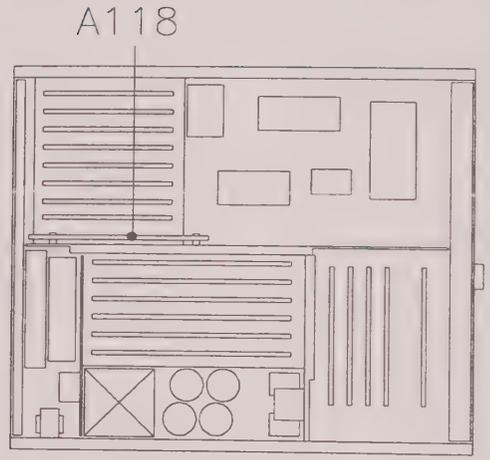
Path switching is accomplished by a control voltage input at J1 (received from the Driver PC board, A14), which biases the diodes CR1 through CR4 in order to activate the desired path. In the Generate mode, the input voltage is negative, turning on diodes CR3 and CR4 and opening a transmission path from J2 to J5. In Track or Manual mode, the control voltage is positive, turning on diodes CR1 and CR2 and opening a transmission path from J2 to J4.

A low pass filter is included in the Track/Manual transmission path (see L1, L2, etc). This filter can be programmed by the computer, in order to increase or decrease the rolloff point. When the voltage control input at P1 turns Q1 on, the shunt capacitor C7 is added to the filter circuit, rolling off the IF output more sharply. The frequency counter circuit uses alternate filter profiles for sideband identification.



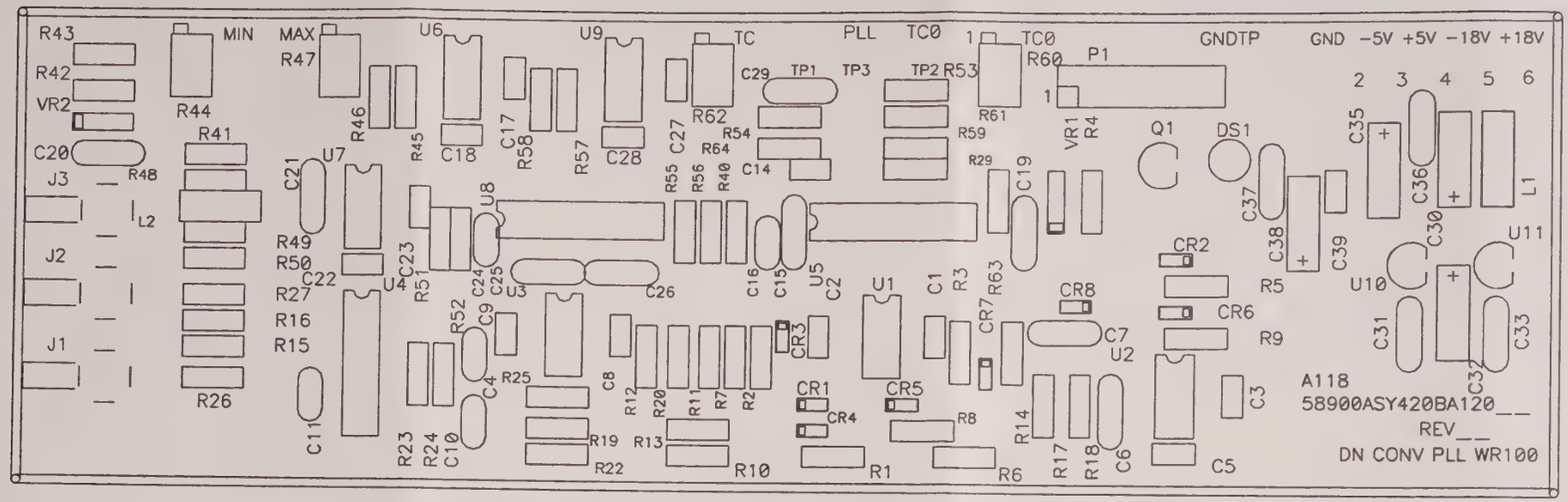
NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF.
2. RESISTORS ARE 1/5W,1%, IN OHMS.
3. * INDICATES CHIP CAP.



Downconverter PLL (A118)

DWG# 420BM12000 Rev D



DOWNCONVERTER PLL -- PC ASSY A118

The function of this circuit is to tune the instrument's downconverter VCO. Although the circuit produces a single tuning output, this output is a composite of various tuning and correction signals.

U5, a multiplying DAC, generates the basic tuning voltage for the VCO. Its output is based on a reference voltage (+6.2V) regulated by VR1. This voltage is multiplied by a factor which is programmed by the computer to achieve the desired downconverter frequency. The tuning voltage is amplified and inverted by U6 and furnished to the summing junction of the output amplifier (U7-2). R44 and R47, the MIN and MAX pots, allow for calibration of the output at the extremes of the VCO's frequency range.

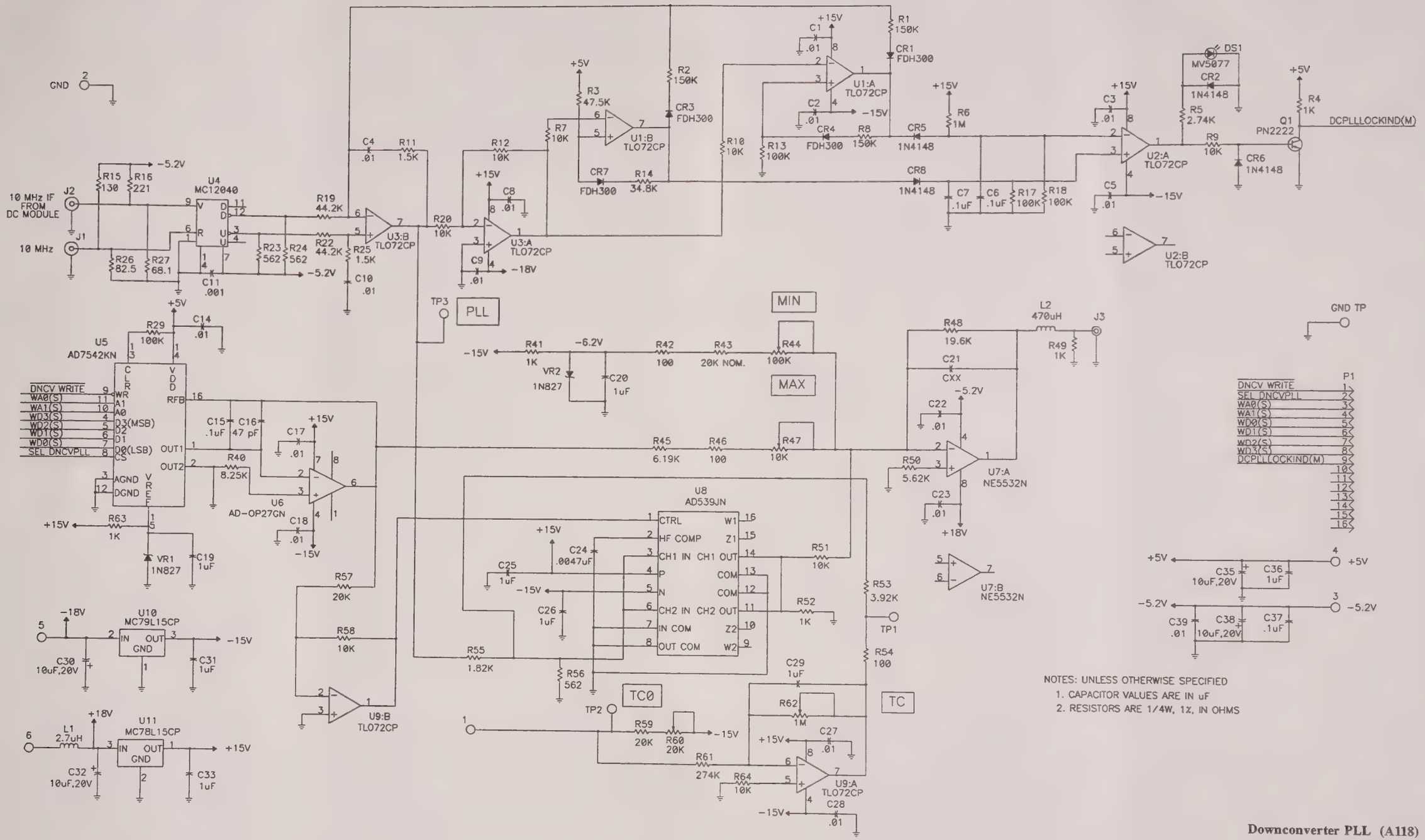
The downconverter VCO is a nonlinear device; its tuning sensitivity varies for different parts of its frequency range. In programming the DAC, the computer takes this nonlinearity into account. However, other elements of the composite tuning output must be corrected for VCO nonlinearity.

The other inputs to the summing junction of U7A are provided through U8, a multiple-input voltage multiplier. The control input to the multiplier comes from U6, by way of the buffer amplifier U9B. The basic tuning voltage from U6-6 is used as the control voltage, so that it serves as a correction factor for VCO nonlinearity. The typical range of this tuning voltage is roughly -1.5V (fMIN) to -6V (fMAX). The other inputs to U8 come from the temperature compensation circuit and the phase lock loop circuit. Both these inputs are combined at U8-3.

Temperature compensation is needed because the frequency of the VCO varies inversely with temperature. The resistance of the temperature compensation resistor on the Downconverter L.O. board (A200A1) decreases as temperature increases, with the result that the input voltage at TP2 rises as the temperature rises. This is inverted and amplified by U9A; the output to U8-3 is a voltage which decreases as temperature increases (the voltage at TP1 will be close to zero volts at room temperature).

The phase lock loop circuit consists of a phase comparator (U4) which receives two 10 MHz inputs. The input at J1 is the 10 MHz master reference. The input at J2 is the I.F. fed back from the downconverter mixer, which should equal 10 MHz when the loop is locked. The PLL circuit adjusts the tuning output to the downconverter VCO in order to equalize the two inputs to the phase comparator. If the two inputs are out of phase, the comparator produces broad pulses on one of its outputs (pins 3 and 12), depending on whether the variable input is leading or lagging the reference. An amplifier/filter circuit (U3B) converts these pulses into a phase correction voltage which is supplied to U8-3. U1A and U1B are employed as "kicker" circuits; if the amplified correction voltage at U3-1 is pegged at one or the other extreme of its range, the appropriate kicker circuit detects this and briefly drives the voltage to the opposite extreme so that the phase detector can resume frequency searching. An out-of-range phase correction voltage will also trigger the unlock detector circuit consisting of U2A and Q1, causing the LED DS1 to light and the LOCK DNCNV data line to go low.

The phase correction and temperature compensation inputs are combined with the DAC's basic tuning voltage at the summing junction of the output amplifier (U7A, an inverting amplifier) and furnished (through J3) to the downconverter L.O. board. The typical output tuning range is roughly +5V (fMIN) to +14V (fMAX).

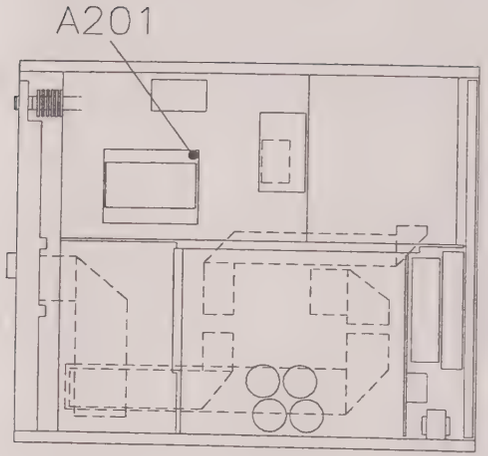


Downconverter PLL (A118)

DWG# 420BM12000 Rev D

Sheet 3 of 3

7-A118-3

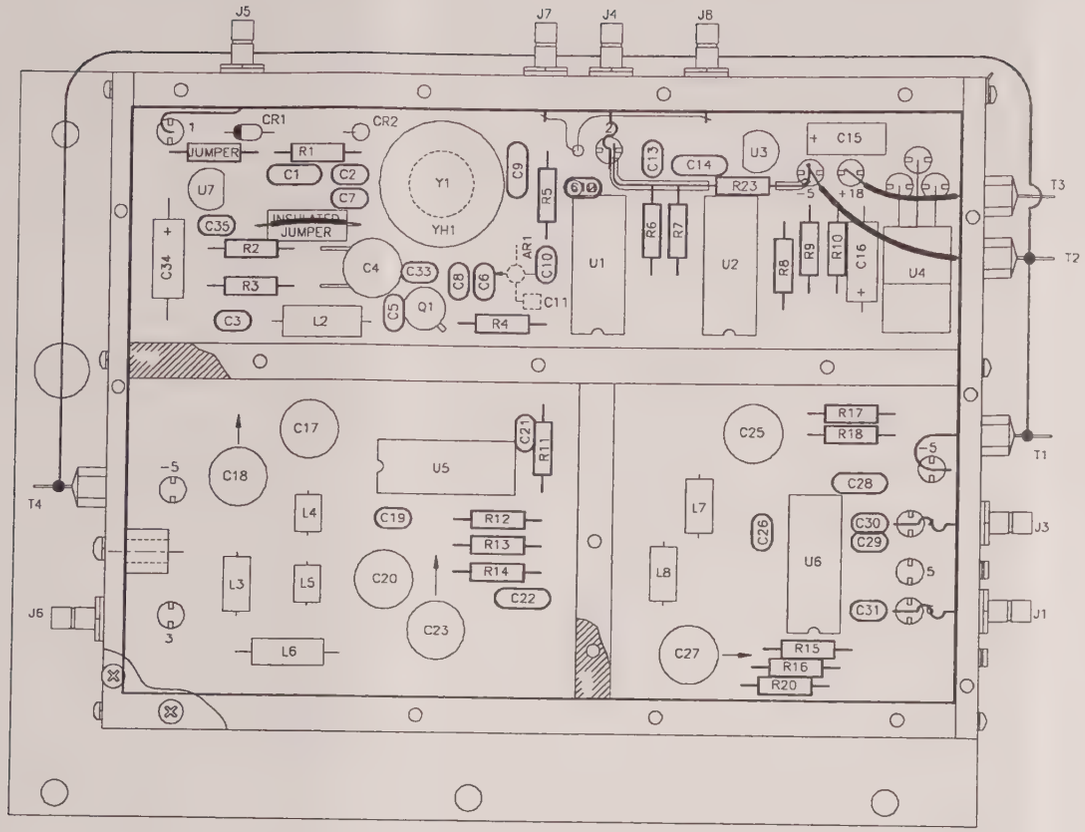


Oscillator/Multiplier (A201)

DWG# 304BM05720 Rev A

Sheet 1 of 3

7-A201-1



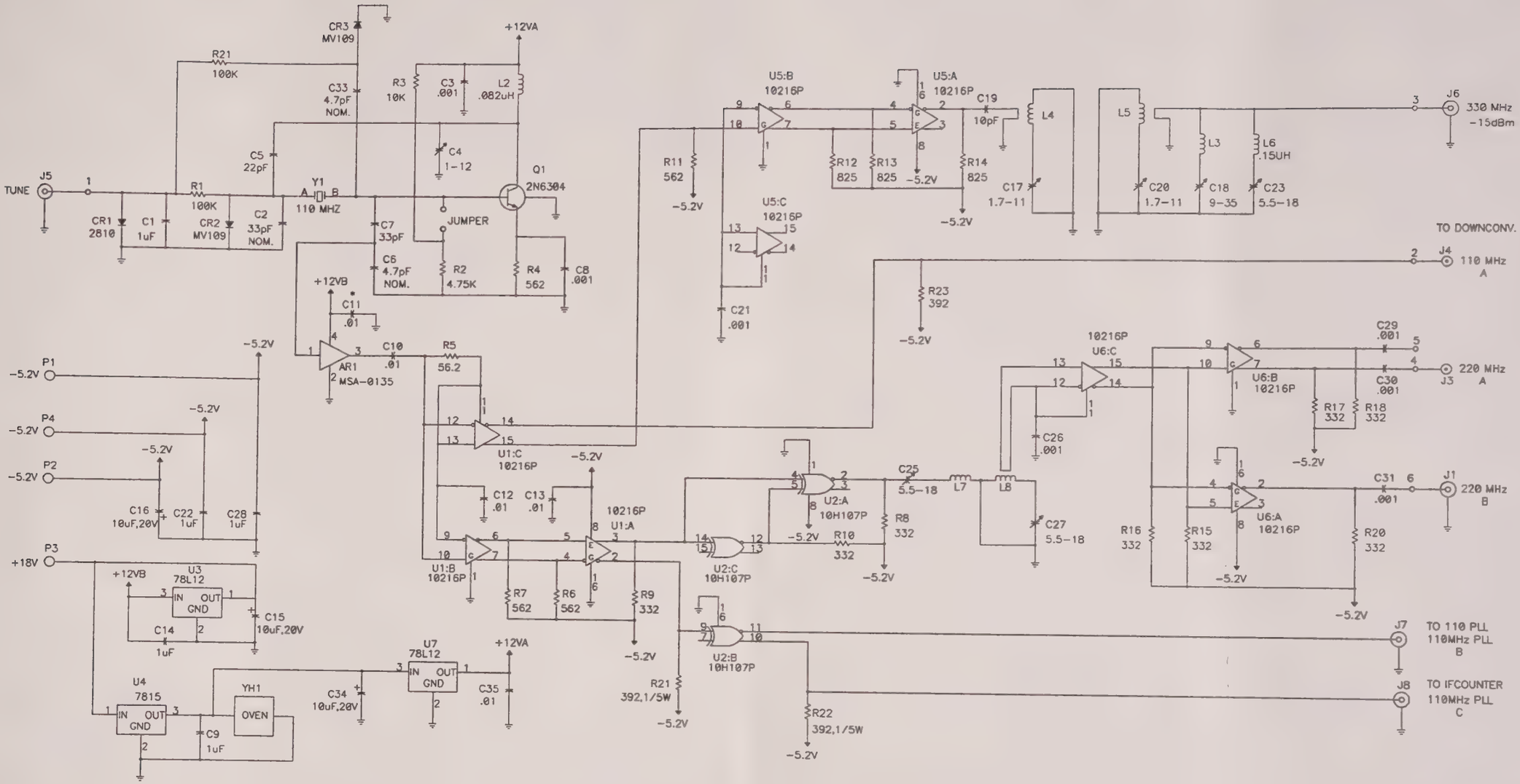
110 MHz OSCILLATOR/MULTIPLIER -- PC ASSY A201

This circuit is the source for the 220 MHz and 330 MHz reference signals used by various phase lock loop circuits in the synthesizer.

The voltage controlled crystal oscillator (Q1, etc.) uses a quartz crystal resonator (Y1); a tuned circuit (L2, etc.) restricts the crystal to an oscillation mode at 110 MHz. The VCXO is fine tuned by a voltage input from the 110 MHz PLL circuit (A12). Its output signal is amplified by AR1 and buffered by line receiver U1:C. The buffered 110 MHz signal is fed back to the PLL and is also furnished to the frequency doubler and frequency tripler.

Two exclusive-NOR gates (U2:A & U2:C) form a frequency doubler (the output toggles on both the leading and trailing edges of the input). The resulting 220 MHz fundamental frequency is inductively coupled to a buffer stage (U6) through a band-pass circuit (L7/L8, etc.). Two trimmer caps (C25 and C27) provide peaking adjustment. The output buffers (U6) provide three samples of this 220 MHz signal to other circuits in the synthesizer.

The frequency tripler takes advantage of the powerful third harmonic component present in any square wave. The line receivers of U5 produce a square 110 MHz signal which is inductively coupled through a band-pass circuit (L4/L5, etc.). The variable capacitors provide peaking adjustment. Two band-stop filters on the output (L3, L6) are used to remove the fundamental and the second harmonic of the VCXO frequency. The 330 MHz output is not buffered, because the circuit to which it is furnished does not require a high power input.



NOTES: UNLESS OTHERWISE SPECIFIED

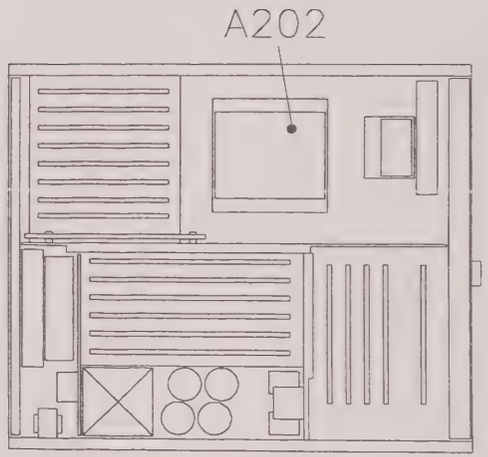
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE 1/4W,1% IN OHMS.
3. " ∘ " INDICATES CHIP CAPACITOR

Oscillator/Multiplier (A201)

DWG# 304BM05720 Rev A

Sheet 3 of 3

7-A201-3

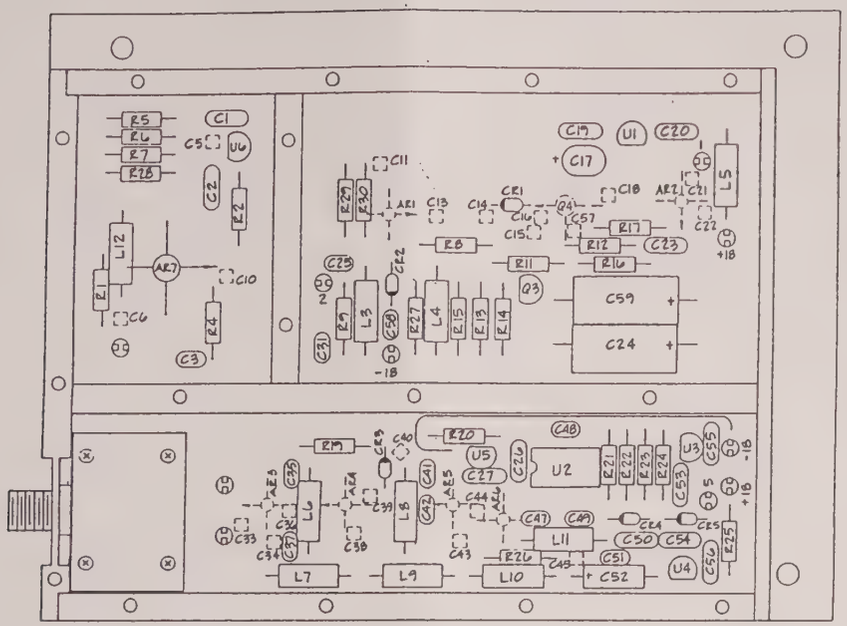


300 MHz Oscillator (A202)

DWG# 304BM05510 Rev B

Sheet 1 of 3

7-A202-1



300 MHz Oscillator (A202)

DWG# 304BM05510 Rev B

Sheet 2 of 3

7-A202-2

300 MHz OSCILLATOR/DRIVER -- PC ASSY A202

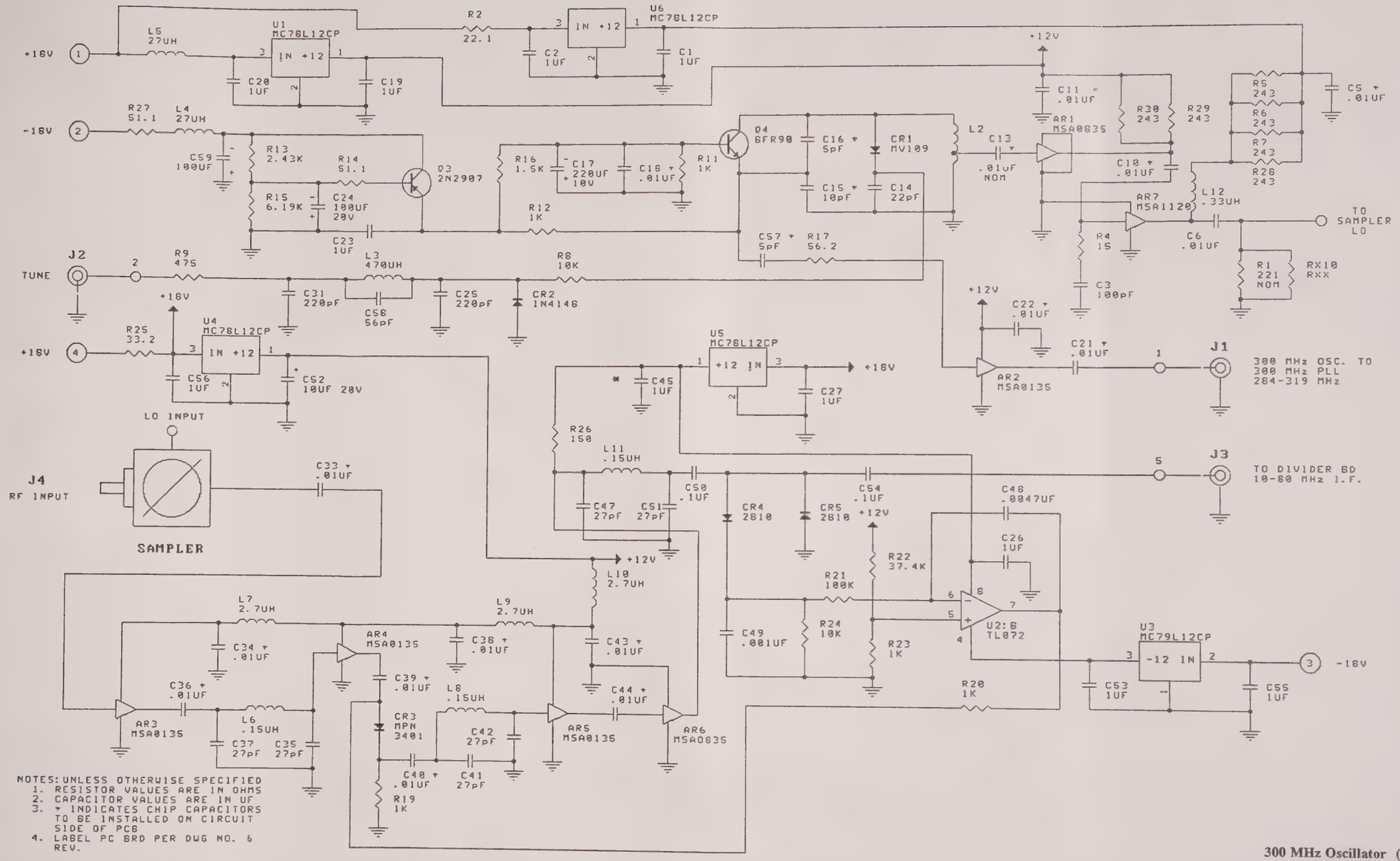
This circuit board is encased in an aluminum housing; it is not normally accessible to service in the field.

The tuning output from the 300 MHz PLL circuit board (A11) is received at J2. A 1 MHz trap (L3, etc.) reduces the reference-frequency component contributed by the PLL's phase detector. The filtered control signal is applied to the voltage-controlled oscillator (Q4). A sample of the VCO frequency is fed back to the PLL circuit (see AR2) in order to permit phase lock. The VCO operates over a range of 284 to 319 MHz.

The VCO output frequency is taken at L2; this inductor is implemented as a conductive strip in the printed circuit artwork and is tapped very close to ground in order to reduce the load on the oscillator and insure stability. The VCO frequency is amplified by AR1 and AR7 to meet the input level requirement of the sampling mixer (about 4 Vpp).

The sampling mixer is a miniature hybrid RF circuit which combines a mixer with a step-recovery diode multiplier. The multiplier (to which the VCO frequency from the driver is applied) generates numerous harmonic multiples of its input frequency. The harmonics are used as one input to the RF mixer; the other input (see J4) is a sample of the YIG oscillator frequency, obtained from a coupler in the RF module. Because one mixer input is a harmonic series, the intermediate frequency output includes numerous sum and difference frequency components.

The mixer IF must be filtered and amplified in order to isolate one IF component in the range of 10-80 MHz. The power level of the IF output is very low; AR3, AR4 and AR5 each provide about +19 dB of gain, and the final amplifier stage (AR6) provides about +33 dB of gain. Three low-pass filters (L6, L8 and L11) roll off sharply above 130 MHz to eliminate harmonics of the IF. The amplitude of the sampling mixer IF is highly variable with frequency; in order to obtain a flat frequency response, an AGC circuit is added (U2-7). Diodes CR4 and CR5 are used by the circuit as signal level detectors; a correction voltage is produced and is applied to attenuator diode CR3 in order to maintain a 1 Vpp IF output at J3.

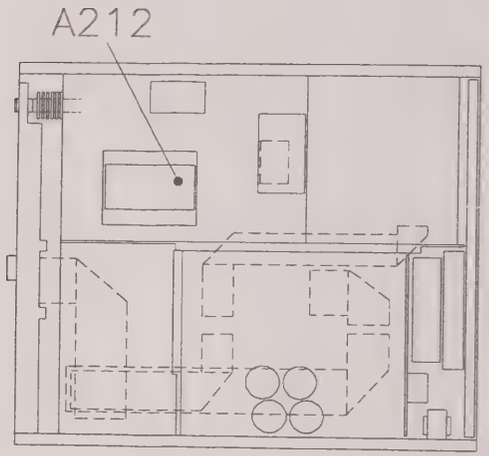


300 MHz Oscillator (A202)

DWG# 304BM05510 Rev B

Sheet 3 of 3

7-A202-3

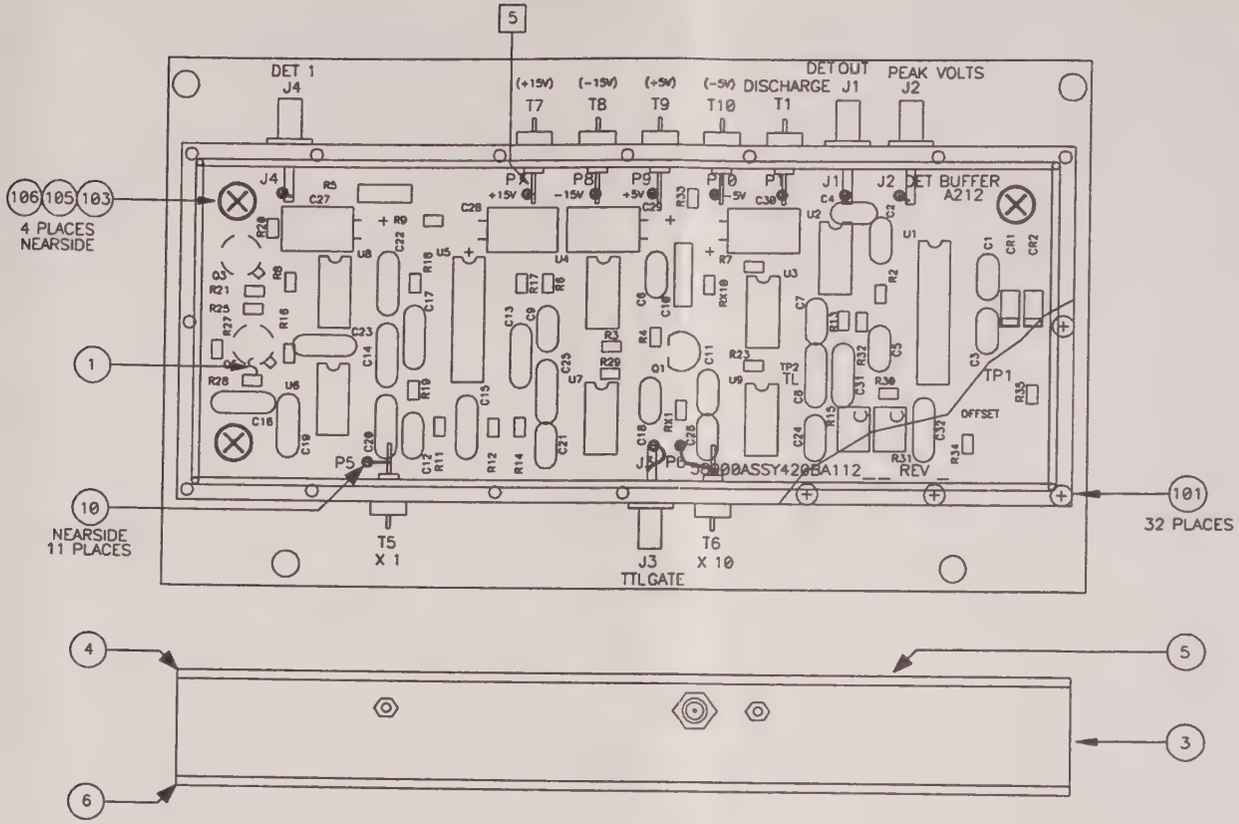


Detector Buffer (A212)

DWG# 420BM11210 Rev B

Sheet 1 of 3

7-A212-1



DETECTOR BUFFER -- PC ASSY A212

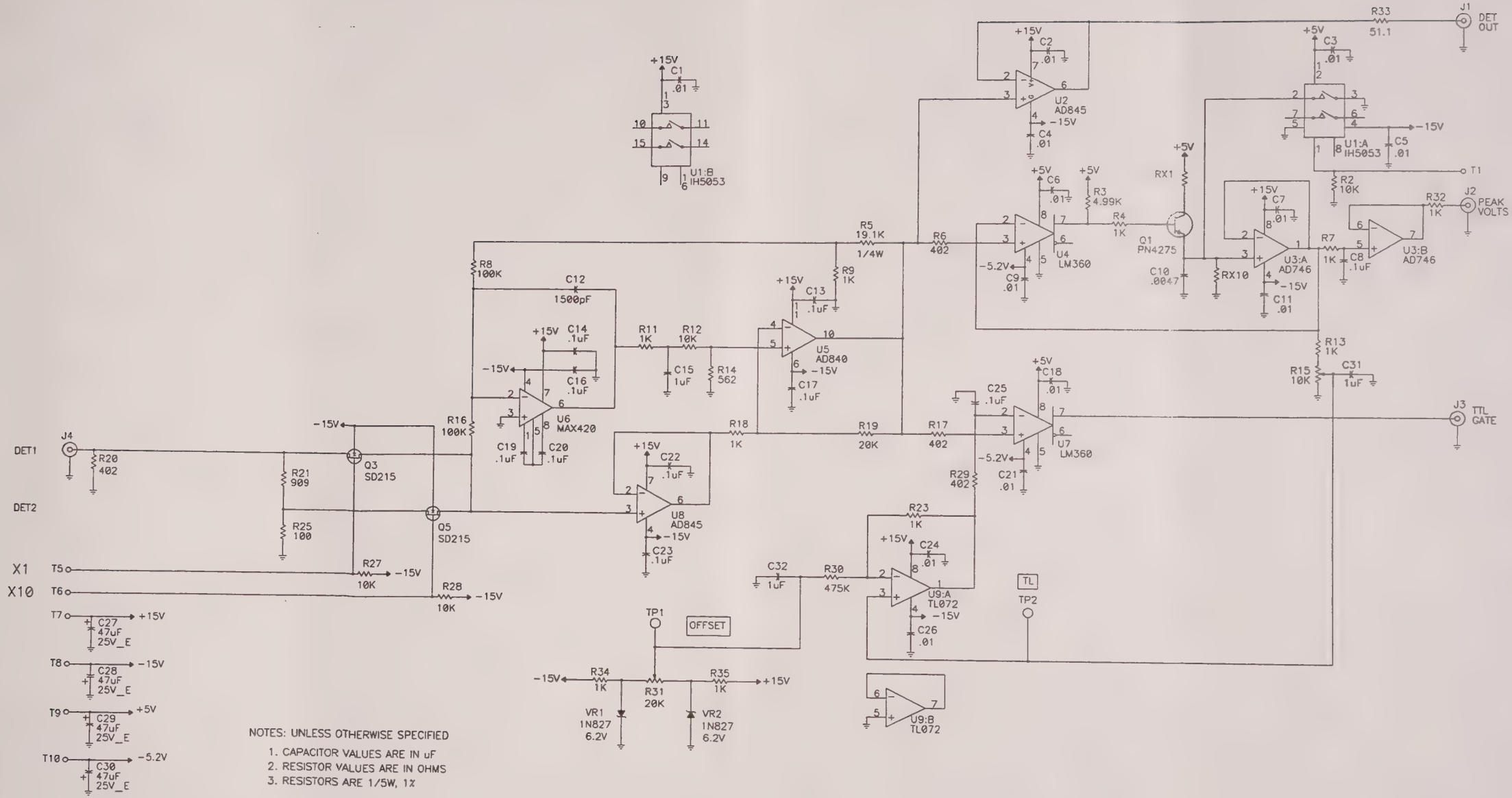
The voltage input from the level detector is received at J4, and passes to the gain stage through one of two FETs (Q3 and Q5). The input paths are selected by the control lines labeled 'X1' and 'X10'. In 'X1' mode, the detector input passes directly through Q3 to the gain stage. In 'X10' mode, the detector input is reduced to one-tenth of its original value by a voltage divider (R21/R25) and passes through Q5 to the gain stage. The 'X10' mode, in which the sensitivity of the power measurement circuit is reduced, is selected automatically by the computer at high input power levels.

The gain stage consisting of U5, U6, and U8 is used to boost the input detector voltage for use by other circuits.

U7 produces an output at TTL voltage levels which signals the presence or absence of a detector input voltage; this is the TTL GATE which is used by the IF Counter circuit board (A18). The trigger level is adjustable, for calibration purposes, by means of the circuit consisting of U9A, R31 (the offset pot) and R15 (the gain pot).

U2 provides a buffered detector output at J1 for the front panel 'DET OUT' connector.

U4, Q1, U3A, U3B, and U1A constitute a sample-and-hold circuit for the detector input; this allows for a steady detector reading of a pulsed RF input. C10 is charged up to the level of the detector signal when it is present; this peak voltage is furnished, through U3A and U3B, to J2. This PEAK VOLTS output is used by the PRF A/D Peak Detector circuit (A17). At intervals, the computer discharges C10 by closing the switch U1A, grounding the capacitor.



NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W, 1%

Detector Buffer (A212)

DWG# 420BM11210 Rev B

Sheet 3 of 3

7-A212-3

8 Options

As of the printing date, no options are available for the WR-100 Series.

9 Special Configurations

The instrument for which this manual is supplied includes no special modifications.

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